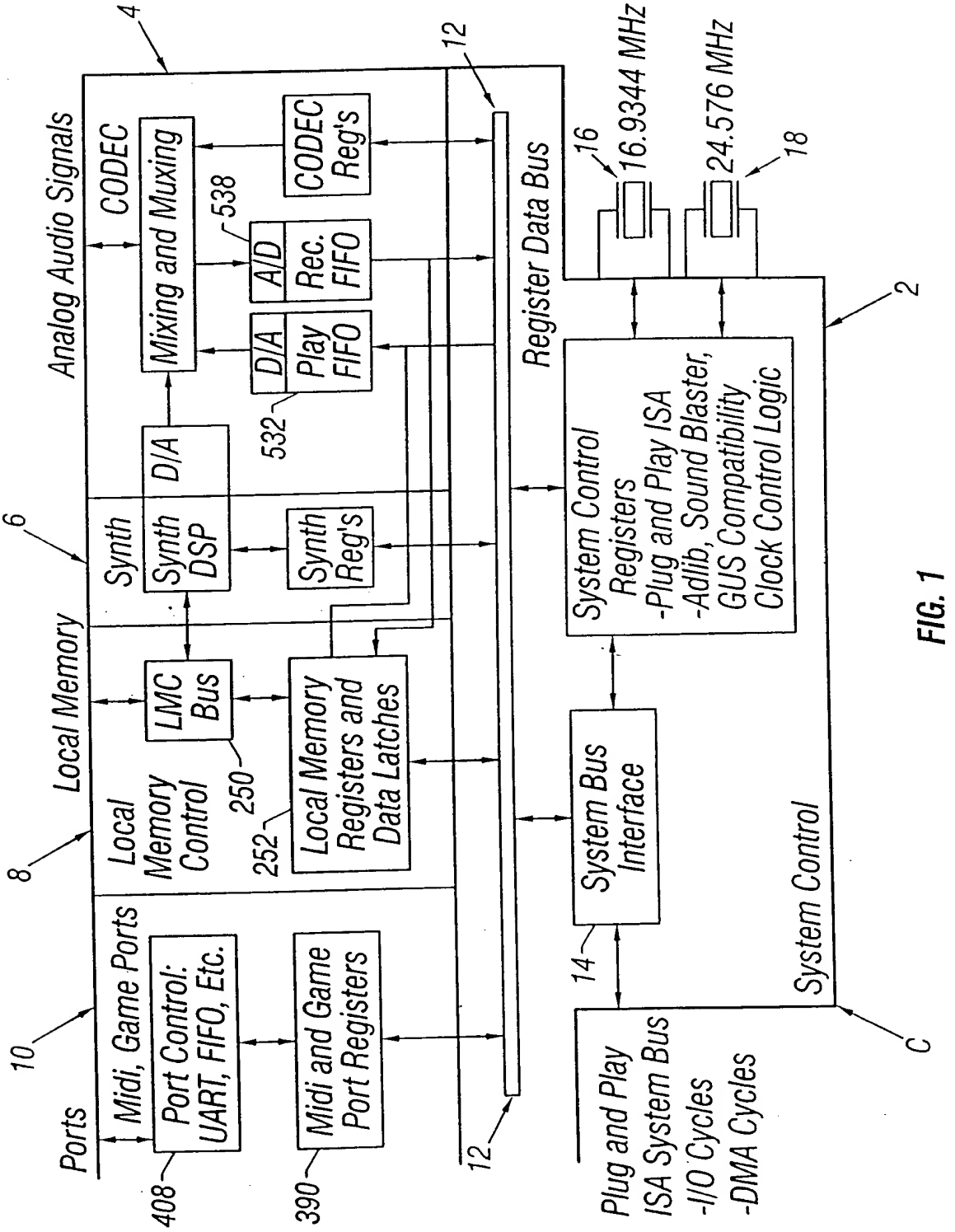


FIG. 1

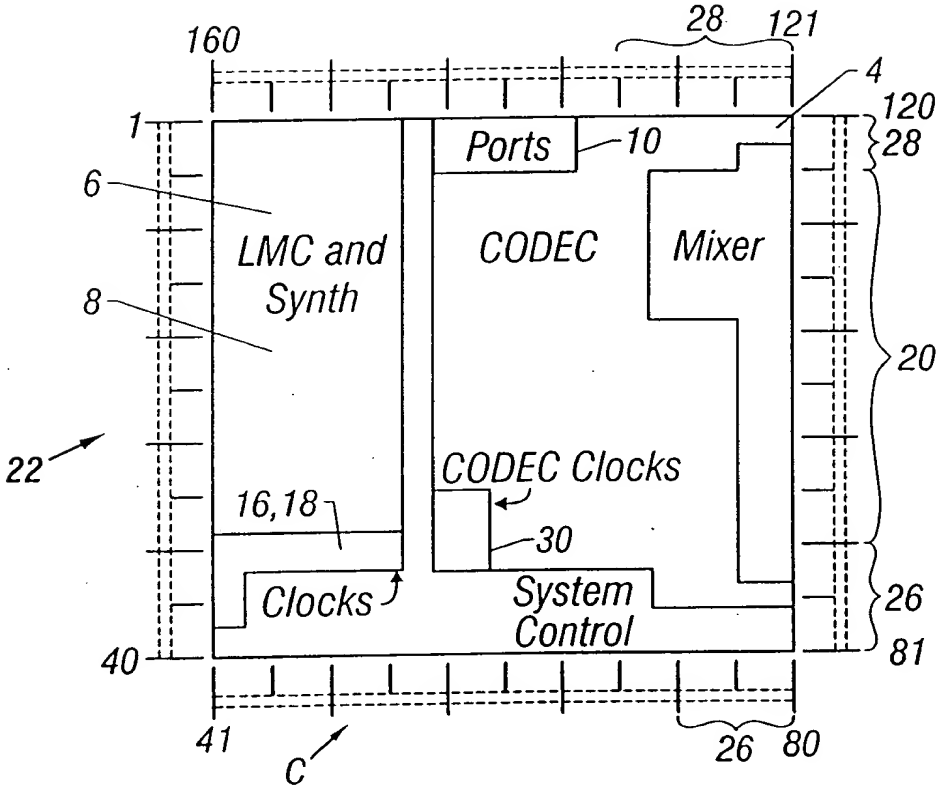

160
28
121
4
120
28
1
Ports
10
6
LMC and
Synth
CODEC
Mixer
8
20
22
CODEC Clocks
16,18
30
Clocks
System
Control
26
81
40
41
C
26
80

FIG. 2

Pin	Signal Name	Pin	Signal Name
1	MA[9]	41	RA[21]
2	VSS	42	RA[20]
3	CD_IRQ	43	SD[0]
4	MA[8]	44	SD[15]
5	MA[7]	45	VSS
6	MA[6]	46	DRQ[0]
7	CD_DRQ	47	SD[1]
8	VSS	48	SD[14]
9	MA[5]	49	VCC
10	MA[4]	50	DAK[0]#
11	CD_DAK#	51	SD[2]
12	MA[3]	52	SD[13]
13	MA[2]	53	VSS
14	VCC	54	IRQ[3]
15	CD_CS#	55	SD[3]
16	MA[1]	56	SD[12]
17	MA[0]	57	VCC
18	BKSEL[3]#	58	IRQ[5]
19	BKSEL[2]#	59	SD[4]
20	VSS	60	SD[11]
21	BKSEL[1]#	61	VSS
22	BKSEL[0]#	62	SD[5]
23	DRQ[7]	63	SD[10]
24	DAK[7]#	64	TC
25	ROMCS#	65	VSS
26	RAHLD#	66	SD[6]
27	RAS#	67	SD[9]
28	MWE#	68	IOR#
29	IVCC	69	VCC
30	IVSS	70	SD[7]
31	DRQ[6]	71	SD[8]
32	DAK[6]#	72	IOW#
33	VSS	73	AEN
34	XTAL2I	74	IOCHRDY
35	XTAL2O	75	IOCS16#
36	XTAL1I	76	IOCHK#
37	XTAL1O	77	VSS
38	VCC	78	IRQ[7]
39	DAK[5]#	79	IRQ[2]
40	DRQ[5]	80	DRQ[1]

FIG. 3A

Pin	Signal Name	Pin	Signal Name
81	DAK[1]#	121	GAMIN[0]
82	SA[8]	122	SA[7]
83	SA[9]	123	SA[6]
84	SA[10]	124	SA[5]
85	SA[11]	125	SA[4]
86	GPOUT[1]	126	SA[3]
87	AVSS	127	SA[2]
88	AVCC	128	SA[1]
89	AVSS	129	SA[0]
90	IREF	130	SBHE#
91	PNPCS	131	GAMIN[3]
92	CFILT	132	GAMIN[2]
93	AVSS	133	MIDIRX
94	AVCC	134	MIDITX
95	AREF	135	DAK[3]#
96	AUX1[L]	136	DRQ[3]
97	MIC[L]	137	IVSS
98	AVSS	138	IVCC
99	AVCC	139	SUSPEND#
100	MIC[R]	140	C32KHZ
101	AUX1[R]	141	GAMIO[0]
102	AUX2[L]	142	VSS
103	LINEIN[L]	143	GAMIO[1]
104	LINEIN[R]	144	GAMIO[2]
105	AUX2R	145	VCC
106	AVSS	146	MD[7]
107	AVSS	147	MD[6]
108	AVCC	148	MD[5]
109	LINEOUT[L]	149	GAMIO[3]
110	LINEOUT[R]	150	VSS
111	AVSS	151	MD[4]
112	MONOOUT	152	IRQ[11]
113	MONOIN	153	IRQ[12]
114	AVSS	154	MD[3]
115	AVCC	155	VCC
116	AVCC	156	MD[2]
117	AVSS	157	MD[1]
118	GPOUT[0]	158	MD[0]
119	RESET	159	IRQ[15]
120	GAMIN[1]	160	MA[10]

FIG. 3B

Pin	Signal Name	Pin	Signal Name
1	SA[7]	41	EX_DRQ
2	SA[8]	42	GAMIN[3]
3	GPOUT[0]	43	GAMIN[2]
4	RESET	44	GAMIN[1]
5	GPOUT[1]	45	GAMIN[0]
6	VCC	46	GAMIO[3]
7	AVSS	47	GAMIO[2]
8	AVSS	48	GAMIO[1]
9	IREF	49	GAMIO[0]
10	CFILT	50	IVSS
11	AVSS	51	VSS
12	AVCC	52	MA[0]
13	AREF	53	MA[1]
14	AUX1[L]	54	EX_DAK#
15	MIC[L]	55	VCC
16	AVSS	56	MA[2]
17	AVCC	57	MA[3]
18	AVSS	58	MA[4]
19	AUX1[R]	59	MA[5]
20	MIC[R]	60	EX_IRQ
21	AUX2[R]	61	EX_CS#
22	LINEIN[R]	62	VSS
23	AVSS	63	MA[6]
24	LINEIN1[L]	64	MA[7]
25	AUX2[L]	65	MA[8]
26	AVCC	66	MA[9]
27	LINEOUT[R]	67	MA[10]
28	AVSS	68	DAK[5]#
29	LINEOUT[L]	69	MD[0]
30	MONOOUT	70	MD[1]
31	MONOIN	71	MD[2]
32	AVSS	72	MD[3]
33	AVCC	73	VSS
34	AVSS	74	DRQ[5]
35	PNPCS	75	VCC
36	SA[9]	76	DAK[6]#
37	SA[10]	77	DRQ[6]
38	SA[11]	78	MD[4]
39	VCC	79	MD[5]
40	VSS	80	MD[6]

FIG. 4A

Pin	Signal Name	Pin	Signal Name
81	MD[7]	121	SD[11]
82	IVCC	122	SD[10]
83	DRQ[7]	123	SD[9]
84	DAK[7]#	124	SD[8]
85	ROMCS#	125	TC
86	RAHLD#	126	DRQ[1]
87	RAS#	127	DAK[1]#
88	MWE#	128	AEN
89	RA[20]	129	IOCHRDY
90	RA[21]	130	IRQ[2]
91	VCC	131	IRQ[3]
92	IRQ[15]	132	IOR#
93	IRQ[12]	133	VSS
94	BKSEL[0]#	134	VCC
95	BKSEL[1]#	135	IOW#
96	VSS	136	IOCS16#
97	BKSEL[2]#	137	SD[0]
98	BKSEL[3]#	138	SD[1]
99	IRQ[11]	139	SD[2]
100	XTAL1I	140	SD[3]
101	XTAL1O	141	VSS
102	VSS	142	SD[4]
103	XTAL2O	143	SD[5]
104	XTAL2I	144	SD[6]
105	VCC	145	SD[7]
106	MIDIRX	146	VCC
107	MIDITX	147	IVSS
108	C32KHZ	148	IRQ[6]
109	SUSPEND#	149	IRQ[7]
110	VSS	150	IOCHK#
111	SBHE#	151	SA[0]
112	DRQ[0]	152	SA[1]
113	DAK[0]#	153	SA[2]
114	IVCC	154	SA[3]
115	VCC	155	SA[4]
116	SD[15]	156	SA[5]
117	SD[14]	157	VSS
118	SD[13]	158	DRQ[3]
119	SD[12]	159	DAK[3]#
120	VSS	160	SA[6]

FIG. 4B

System Control				Codec		Local Memory		Ports, Misc.		
		pwr & gnd	10	pwr & gnd	15	pwr & gnd	6	pwr & gnd	6	
SD[15:0]	16	IOCS16#	1	MIC[L,R]	2	MA[10:0]	11	XTAL1I	1	
SA[11:0]	12	IOCHRDY	1	AUX1[L,R]	2	MD[7:0]	8	XTAL1O	1	
SBHE#	1	AEN	1	AUX2[L,R]	2	BKSEL[3:0]#	4	XTAL2I	1	
DRQ[7:5,3,1:0]	6	CD_IRQ	1	LINEIN[L,R]	2	ROMCS#	1	XTAL2O	1	
DAK[7:5,3,1:0]#	6	CD_DRQ	1	LINEOUT[L,R]	2	RAHLD#	1	MIDIRX	1	
TC	1	CD_DAK#	1	MONOIN	1	RA[21:20]	2	MIDITX	1	
IRQ[15,12,11]	3	CD_CS#	1	MONOOUT	1	MWE#	1	GAMIN[3:0]	4	
IRQ[7,5,3,2]	4	RESET	1	IREF	1	RAS#	1	GAMIO[3:0]	4	
IOCHK#	1	SUSPEND#	1	CFILT	1	*EFFECT#				
IOR#	1	C32KHZ	1	AREF	1	*FRSYNC#				TOTAL
IOW#	1	PNPCS	1	GPOUT[1:0]	2					
	52		21		32		35		20	160

FIG. 5

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

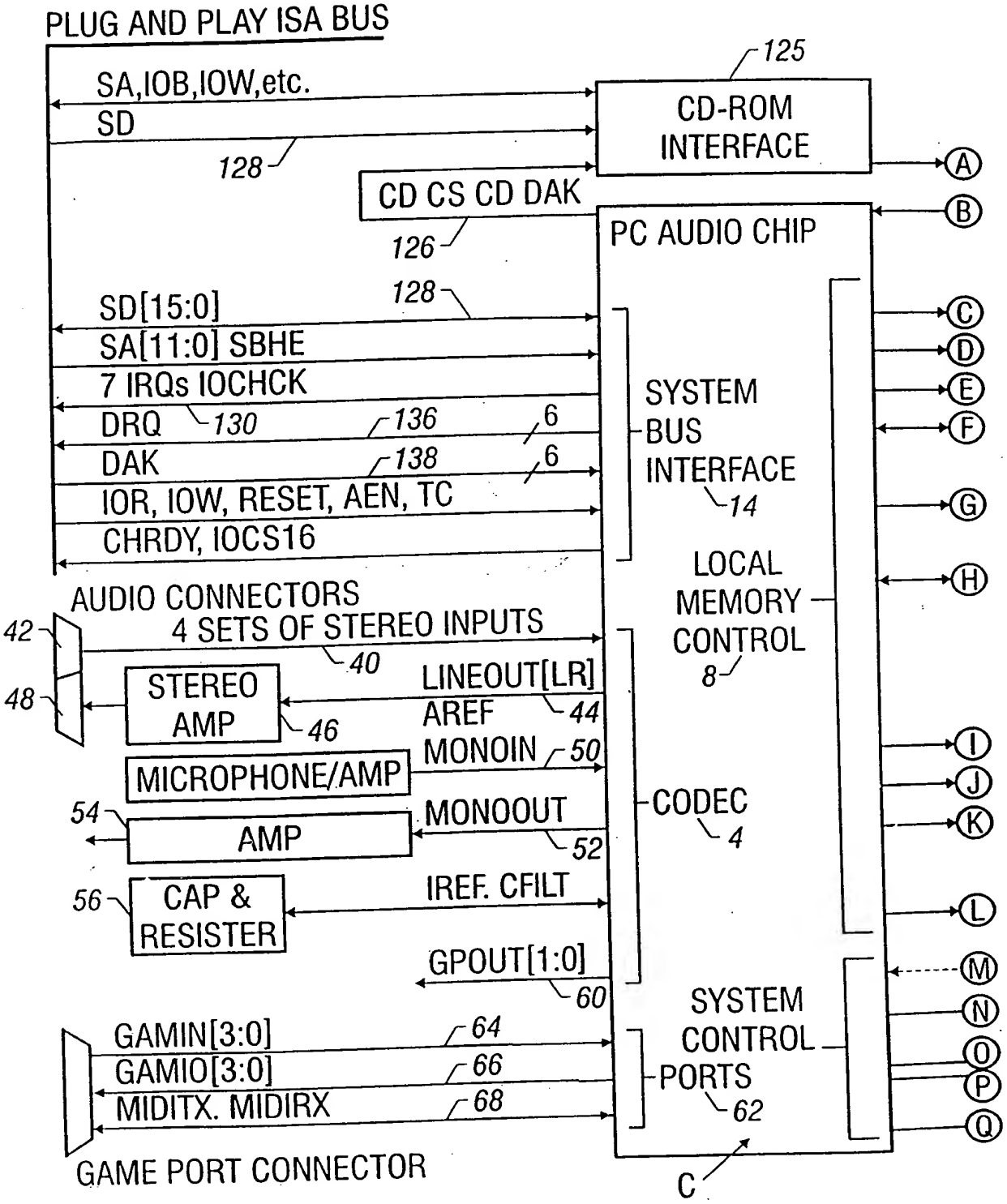

PLUG AND PLAY ISA BUS
SA,IOB,IOW,etc.
SD
128
125
CD-ROM
INTERFACE
A
CD CS CD DAK
126
PC AUDIO CHIP
B
SD[15:0]
SA[11:0] SBHE
7 IRQs IOCHCK
DRQ
130
136
6
DAK
138
6
IOR, IOW, RESET, AEN, TC
CHRDY, IOCS16
SYSTEM
BUS
INTERFACE
14
C
D
E
F
G
H
AUDIO CONNECTORS
42
4 SETS OF STEREO INPUTS
40
48
STEREO
AMP
46
LINEOUT[LR]
AREF
44
MONOIN
50
MICROPHONE/AMP
54
AMP
MONOOUT
52
56
CAP &
RESISTER
IREF. CFILT
GPOUT[1:0]
60
LOCAL
MEMORY
CONTROL
8
CODEC
4
I
J
K
L
M
N
O
P
Q
SYSTEM
CONTROL
PORTS
62
GAMIN[3:0]
64
GAMIO[3:0]
66
MIDITX. MIDIRX
68
GAME PORT CONNECTOR
C

FIG. 6A

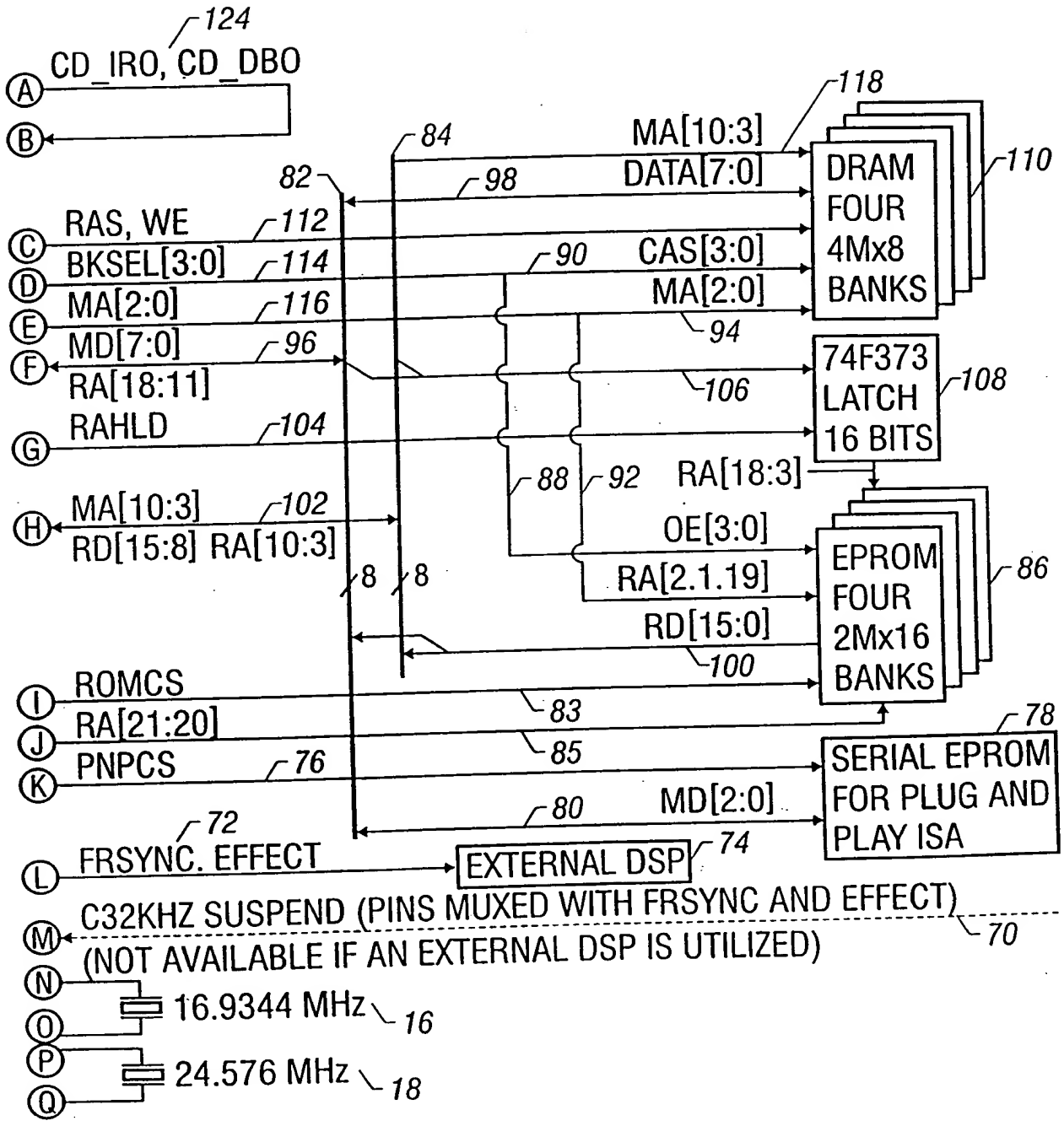

124
CD_IRO, CD_DBO
A
B
84
MA[10:3]
118
82
98
DATA[7:0]
DRAM
FOUR
4Mx8
BANKS
110
RAS, WE
112
C
BKSEL[3:0]
114
D
90
CAS[3:0]
MA[2:0]
E
MA[2:0]
116
94
MD[7:0]
96
F
RA[18:11]
106
74F373
LATCH
16 BITS
108
RAHLD
104
G
88
92
RA[18:3]
MA[10:3]
102
H
RD[15:8] RA[10:3]
OE[3:0]
EPROM
FOUR
2Mx16
BANKS
86
8
8
RA[2.1.19]
RD[15:0]
100
ROMCS
I
83
RA[21:20]
J
85
78
PNPCS
76
K
SERIAL EPROM
FOR PLUG AND
PLAY ISA
80
MD[2:0]
72
FRSYNC. EFFECT
L
EXTERNAL DSP
74
C32KHZ SUSPEND (PINS MUXED WITH FRSYNC AND EFFECT)
M
70
(NOT AVAILABLE IF AN EXTERNAL DSP IS UTILIZED)
N
16.9344 MHz
16
O
P
24.576 MHz
18
Q

FIG. 6B

Name	Qty	Type	Description
BKSEL[3:0]#	4	output	Bank Selects. Used in to control the CAS inputs to each of the DRAM banks or the Output Enable inputs to each of the ROM banks.
C32KHZ / EFFECT#	1	input / output	Based on the power-up state of RA[21], this pin is either a clock input or an output to an external DSP. C32KHZ (RA[21] high) is a 32 KHz clock used in suspend mode to operate the refresh circuitry. EFFECT# (RA[21] low) becomes active during the writes to DRAM that are for the delay-based effects from the synthesizer.
SUSPEND# / FRSYNC#	1	input / output	Based on the power-up state of RA[21], this pin is either an input to cause suspend mode or an output to an external DSP. SUSPEND# (RA[21] high) is a system control signal. FRSYNC# (RA[21] low) becomes active at the beginning of each new frame.
MA[10:3]	8	bi-dir	Memory Address. Are the multiplexed row-column address bits for DRAM cycles. Are the multiplexed RLA[10:3] outputs and D[15:8] inputs for ROM cycles.
MA[2:0]	3	output	Memory Address. Are the multiplexed row-column address bits for DRAM cycles. Are the RLA[2,1,19] outputs for ROM cycles.

FIG. 7A

Name	Qty	Type	Description
MD[7:0]	8	bi-dir	Data Bus. Are the data-bus bits for DRAM cycles. Are the multiplexed RLA[18:11] outputs and D[7:0] inputs for ROM cycles. For serial EEPROM accesses, MD[2] is the clock, SK. MD[1] is DI (serial EEPROM data input). MD[0] is DO (serial EEPROM data output).
MWE#	1	output	Write Enable. Goes to the WE# pin of all the DRAM banks; is high during refresh cycles. During reset, MWE# becomes an input that is used to select between pin options (see PIN SUMMARY in the general description part of this document).
RA[21:20]	2	bi-dir	ROM Address. These outputs provide the ROM address during ROM accesses. During reset, these become inputs that are used to select between pin options; see the PIN SUMMARY section of the general description for details).
RAHLD#	1	output	ROM Address Hold. Used to latch the state of MD[7:0] (RLA[18:11]) and MA[10:3] (RLA[10:3]) in external latches during ROM accesses.
RAS#	1	output	Goes to the RAS# pin of all the DRAM banks.
ROMCS#	1	output	ROM Chip Select. Goes to the CS# input to all the ROM banks.

FIG. 7B

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
UMCR	Mix Control Register	P2XR+0	-	rd-wr	sys con
UISR	IRQ Status Register	P2XR+6	-	read	sys con
U2X6R	Sound Blaster 2x6 Register	P2XR+6	-	write	sys con
UACWR	AdLib Command Write Register	P2XR+8, 388	-	write	sys con
UASRR	AdLib Status Read Register	P2XR+8, 388	-	read	sys con
UADR	AdLib Data Register	P2XR+9, 389	-	rd-wr	sys con
UACRR	AdLib Command Read Register	P2XR+0Ah	-	read	sys con
UASWR	Adlib Status Write Register	P2XR+0Ah	-	write	sys con
UHRDP	GUS Hidden Register Data Port	P2XR+0Bh	-	rd-wr	sys con
UI2XCR	Sound Blaster IRQ 2xC Register	P2XR+0Ch	-	rd-wr	sys con
U2XCR	Sound Blaster 2xC Reg. (no IRQ)	P2XR+0Dh	-	write	sys con
U2XER	Sound Blaster 2xE Register	P2XR+0Eh	-	rd-wr	sys con
URCR	Register Control Register	P2XR+0Fh	-	write	sys con
USRR	Status Read Register	P2XR+0Fh	-	read	sys con
UDCI	DMA Channel Control Register	P2XR+0Bh	UMCR[6]=0,	rd-wr	sys con
			URCR[2:0]=0		
UICI	Interrupt Control Register	P2XR+0Bh	UMCR[6]=1,	rd-wr	sys con
			URCR[2:0]=0		
UGP1I	General Purpose Reg. 1 (Back Door)	P2XR+0Bh	URCR[2:0]=1	rd-wr	sys con
UGP2I	General Purpose Reg. 2 (Back Door)	P2XR+0Bh	URCR[2:0]=2	rd-wr	sys con
UGPA1I	General Purpose Reg. 1 Address	P2XR+0Bh	URCR[2:0]=3	rd-wr	sys con

FIG. 8A

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
UGPA2I	General Purpose Reg. 2 Address	P2XR+0Bh	URCR[2:0]=4	rd-wr	sys con
UCLRII	Clear Interrupt Register	P2XR+0Bh	URCR[2:0]=5	write	sys con
UJMPI	Jumper Register	P2XR+0Bh	URCR[2:0]=6	rd-wr	sys con
UGP1I	Gen. Purp. Reg. 1 (Emulation Addr)	UGPA1I	-	rd-wr	sys con
UGP2I	Gen.Purp. Reg. 2 (Emulation Addr)	UGPA2I	-	rd-wr	sys con
GGCR	Game Control Register	201	-	rd-wr	ports
GMCR	MIDI Control Register	P3XR+0	-	write	ports
GMSR	MIDI Status Register	P3XR+0	-	read	ports
GMTDR	MIDI Transmit Data Register	P3XR+1	-	write	ports
GMRDR	MIDI Receive Data Register	P3XR+1	-	read	ports
SVSR	Synth Voice Select Register	P3XR+2	-	rd-wr	synth
IGIDXR	General Index Register	P3XR+3	-	rd-wr	sys con
I16DP	General 16-bit I/O Data Port	P3XR+(4-5)	-	rd-wr	sys con
I8DP	General 8-bit I/O Data Port	P3XR+5	-	rd-wr	sys con
SACI	Synth Address Control (1 per voice)	P3XR+5	IGIDXR=0,80	wr,rd	synth
SFCI	Synth Frequency Control (1 per voice)	P3XR+(4-5)	IGIDXR=1,81	wr,rd	synth
				wr,rd	synth
SASHI	Synth Addr. Start High (1 per voice)	P3XR+(4-5)	IGIDXR=2,82	wr,rd	synth
SASLI	Synth Addr. Start Low (1 per voice)	P3XR+(4-5)	IGIDXR=3,83	wr,rd	synth
SAEHI	Synth Addr. End High (1 per voice)	P3XR+(4-5)	IGIDXR=4,84	wr,rd	synth
SAELI	Synth Addr. End Low (1 per voice)	P3XR+(4-5)	IGIDXR=5,85	wr,rd	synth

FIG. 8B

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
SVRI	Synth Volume Rate (1 per voice)	P3XR+5	IGIDXR=6,86	wr,rd	synth
SVSI	Synth Volume Start(1 per voice)	P3XR+5	IGIDXR=7,87	wr,rd	synth
SVEI	Synth Volume End(1 per voice)	P3XR+5	IGIDXR=8,88	wr,rd	synth
SVLI	Synth Volume Level(1 per voice)	P3XR+(4-5)	IGIDXR=9,89	wr,rd	synth
SAHI	Synth Address High (1 per voice)	P3XR+(4-5)	IGIDXR=A,8A	wr,rd	synth
SALI	Synth Address Low (1 per voice)	P3XR+(4-5)	IGIDXR=B,8B	wr,rd	synth
SROI	Synth Right Offset (1 per voice)	P3XR+(4-5)	IGIDXR=C,8C	wr,rd	synth
SVCI	Synth Volume Control(1 per voice)	P3XR+5	IGIDXR=D,8D	wr,rd	synth
SAVI	Synth Active Voices	P3XR+5	IGIDXR=E,8E	wr,rd	synth
SVII	Synth Voice IRQ	P3XR+5	IGIDXR=8F	read	synth
SUAI	Synth Upper Address (1 per voice)	P3XR+5	IGIDXR=10,90	wr,rd	synth
SEAHI	Synth Effect Addr High (1 per voice)	P3XR+(4-5)	IGIDXR=11,91	wr,rd	synth
SEALI	Synth Effect Addr Low (1 per voice)	P3XR+(4-5)	IGIDXR=12,92	wr,rd	synth
SLOI	Synth Left Offset (1 per voice)	P3XR+(4-5)	IGIDXR=13,93	wr,rd	synth

FIG. 8C

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
SEASI	Synth Effect Accum Sel (1 per voice)	P3XR+5	IGIDXR=14,94	wr, rd	synth
SMSI	Synth Mode Select (1 per voice)	P3XR+5	IGIDXR=15,95	wr, rd	synth
SEVI	Synth Effect Volume (1 per voice)	P3XR+(4-5)	IGIDXR=16,96	wr, rd	synth
SFLFOI	Synth Frequency LFO (1 per voice)	P3XR+5	IGIDXR=17,97	wr, rd	synth
SVLFOI	Synth Volume LFO (1 per voice)	P3XR+5	IGIDXR=18,98	wr, rd	synth
SGMI	Synth Global Mode	P3XR+5	IGIDXR=19,99	wr, rd	synth
SLFOBI	Synth LFO Base Address	P3XR+(4-5)	IGIDXR=1A,9A	wr, rd	synth
SROFI	Synth Right Offset Final (1 per voice)	P3XR+(4-5)	IGIDXR=1B,9B	wr, rd	synth
SLOFI	Synth Left Offset Final (1 per voice)	P3XR+(4-5)	IGIDXR=1C,9C	wr, rd	synth
SEVFI	Synth Effect Vol. Final (1 per voice)	P3XR+(4-5)	IGIDXR=1D,9D	wr, rd	synth
SVIRI	Synth Voice Read IRQ	P3XR+5	IGIDXR=9F	read	synth
LDMACI	LMC DMA Control	P3XR+5	IGIDXR=41	rd-wr	lmc
LDSALI	LMC DMA Start Address[19:4]	P3XR+(4-5)	IGIDXR=42	rd-wr	lmc
LMALI	LMC I/O Address Low[15:0]	P3XR+(4-5)	IGIDXR=43	rd-wr	lmc
LMAHI	LMC I/O Address High[23:16]	P3XR+5	IGIDXR=44	rd-wr	lmc
UASBCI	AdLib-Sound Blaster Control	P3XR+5	IGIDXR=45	rd-wr	sys con
UAT1I	AdLib Timer1 Count	P3XR+5	IGIDXR=46	rd-wr	sys con
UAT2I	AdLib Timer2 Count	P3XR+5	IGIDXR=47	rd-wr	sys con
XXXX	ADC sample rate--no longer used	P3XR+5	IGIDXR=48	write	synth
XXXX	ADC control reg--no longer used	P3XR+5	IGIDXR=49	rd-wr	synth
GJTDI	Joystick Trim DAC	P3XR+5	IGIDXR=4B	rd-wr	port

FIG. 9A

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
URSTI	Reset Register	P3XR+5	IGIDXR=4C	rd-wr	sys con
LDSAHI	LMC DMA Start Addr[23:20], [3:0]	P3XR+5	IGIDXR=50	rd-wr	lmc
LMSBAI	LMC 16-Bit Access Register	P3XR+(4-5)	IGIDXR=51	rd-wr	lmc
LMCFI	LMC Configuration Register	P3XR+(4-5)	IGIDXR=52	rd-wr	lmc
LMCI	LMC Control Register	P3XR+5	IGIDXR=53	rd-wr	lmc
LMRFAI	LMC Record FIFO Base Addr[23:8]	P3XR+(4-5)	IGIDXR=54	rd-wr	lmc
LMPFAI	LMC Play FIFO Base Addr[23:8]	P3XR+(4-5)	IGIDXR=55	rd-wr	lmc
LMFSI	LMC FIFO Size	P3XR+(4-5)	IGIDXR=56	rd-wr	lmc
LDICI	LMC DMA Interleave Control	P3XR+(4-5)	IGIDXR=57	rd-wr	lmc
LDIBI	LMC DMA Interleave Base A[23:8]	P3XR+(4-5)	IGIDXR=58	rd-wr	lmc
ICMPTI	Compatibility Register	P3XR+5	IGIDXR=59	rd-wr	sys con
IDECI	Decode Control Register	P3XR+5	IGIDXR=5A	rd-wr	sys con
IVERI	Version Number Register	P3XR+5	IGIDXR=5B	rd-wr	sys con
IEMUAI	Emulation Register A	P3XR+5	IGIDXR=5C	rd-wr	sys con
IEMUBI	Emulation Register B	P3XR+5	IGIDXR=5D	rd-wr	sys con
GMRFAI	MIDI Receive FIFO Access Reg.	P3XR+5	IGIDXR=5E	write	sys con
ITCI	Test Control Register	P3XR+5	IGIDXR=5F	rd-wr	sys con
UCCDR	Codec/CD-ROM--no longer used	P3XR+6	-	write	sys con
LMBDR	LMC Byte Data	P3XR+7	-	rd-wr	lmc
CIDXR	Codec Index Address Register	PCODAR+0	-	rd-wr	codec
CDATAP	Codec Indexed Data Port	PCODAR+1	-	rd-wr	codec

FIG. 9B

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
CSR1R	Codec Status Register 1	PCODAR+2	-	read	codec
CPDR	Playback Data Register	PCODAR+3	-	write	codec
CRDR	Record Data Register	PCODAR+3	-	read	codec
CLICI	Left A/D Input Control	PCODAR+1	CIDXR[4:0]=0	rd-wr	codec
CRICI	Right A/D Input Control	PCODAR+1	CIDXR[4:0]=1	rd-wr	codec
CLAX1I	Left Aux 1/Synth Input Control	PCODAR+1	CIDXR[4:0]=2	rd-wr	codec
CRAX1I	Right Aux 1/Synth Input Control	PCODAR+1	CIDXR[4:0]=3	rd-wr	codec
CLAX2I	Left Auxiliary 2 Input Control	PCODAR+1	CIDXR[4:0]=4	rd-wr	codec
CRAX2I	Right Auxiliary 2 Input Control	PCODAR+1	CIDXR[4:0]=5	rd-wr	codec
CLDACI	Left DAC Control	PCODAR+1	CIDXR[4:0]=6	rd-wr	codec
CRDACI	Right DAC Control	PCODAR+1	CIDXR[4:0]=7	rd-wr	codec
CPDFI	Playback Data Format	PCODAR+1	CIDXR[4:0]=8	rd-wr	codec
CFIG1I	Configuration Register 1	PCODAR+1	CIDXR[4:0]=9	rd-wr	codec
CEXTI	External Control	PCODAR+1	CIDXR[4:0]=A	rd-wr	codec
CSR2I	Status Register 2	PCODAR+1	CIDXR[4:0]=B	read	codec
CMODEI	Mode Select, ID	PCODAR+1	CIDXR[4:0]=C	rd-wr	codec
CLCI	Loopback Control	PCODAR+1	CIDXR[4:0]=D	rd-wr	codec

FIG. 9C

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
CUPCTI	Upper Playback Count	PCODAR+1	CIDXR[4:0]=E	rd-wr	codec
CLPCTI	Lower Playback Count	PCODAR+1	CIDXR[4:0]=F	rd-wr	codec
CFIG2I	Configuration Register 2	PCODAR+1	CIDXR[4:0]=10	rd-wr	codec
CFIG3I	Configuration Register 3	PCODAR+1	CIDXR[4:0]=11	rd-wr	codec
CLLICI	Left Line Input Control	PCODAR+1	CIDXR[4:0]=12	rd-wr	codec
CRLICI	Right Line Input Control	PCODAR+1	CIDXR[4:0]=13	rd-wr	codec
CUTIMI	Upper Timer	PCODAR+1	CIDXR[4:0]=14	rd-wr	codec
CLTIMI	Lower Timer	PCODAR+1	CIDXR[4:0]=15	rd-wr	codec
CLMICI	Left Microphone Input Control	PCODAR+1	CIDXR[4:0]=16	rd-wr	codec
CRMICI	Right Microphone Input Control	PCODAR+1	CIDXR[4:0]=17	rd-wr	codec
CSR3I	Status Register 3	PCODAR+1	CIDXR[4:0]=18	rd-wr	codec
CLOAI	Left Output Attenuation	PCODAR+1	CIDXR[4:0]=19	rd-wr	codec
CMONOI	Mono Input And Output Control	PCODAR+1	CIDXR[4:0]=1A	rd-wr	codec
CROAI	Right Output Attenuation	PCODAR+1	CIDXR[4:0]=1B	rd-wr	codec
CRDFI	Record Data Format	PCODAR+1	CIDXR[4:0]=1C	rd-wr	codec
CPVFI	Playback Variable Frequency	PCODAR+1	CIDXR[4:0]=1D	rd-wr	codec
CURCTI	Upper Record Count	PCODAR+1	CIDXR[4:0]=1E	rd-wr	codec
CLRCTI	Lower Record Count	PCODAR+1	CIDXR[4:0]=1F	rd-wr	codec
PCSNBR	Card Select Number Back Door	201	-	rd-wr	sys con
PIDXR	Plug And Play Index Addr. Register	279	-	write	sys con
PNPWRP	Plug And Play Write Port	A79	-	write	sys con

FIG. 10A

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
PNPRDP	Plug And Play Read Data Port	PNPRDP	-	read	sys con
PSRPAI	PNP Set PNPRDP Address	A79	279=00	write	sys con
PISOCI	PNP Isolate Command	PNPRDP	279=01	read	sys con
PCCCI	PNP Configuration Control Cmd.	A79	279=02	write	sys con
PWAKEI	PNP Wake[CSN] Command	A79	279=03	write	sys con
PRESDI	PNP Resource Data Register	PNPRDP	279=04	read	sys con
PRESSI	PNP Resource Data Status	PNPRDP	279=05	read	sys con
PCSNI	PCP Card Select Number	PNPRDP, A79	279=06	rd-wr	sys con
PLDNI	PNP Logical Device Number (LDN)	PNPRDP, A79	279=07	rd-wr	sys con
PUACTI	PNP Audio Activate Register	PNPRDP, A79	LDN=0,279=30	rd-wr	sys con
PURCI	PNP Audio I/O Range Check	PNPRDP, A79	LDN=0,279=31	rd-wr	sys con
P2X0HI	PNP set P2xr[9:8]	PNPRDP, A79	LDN=0,279=60	rd-wr	sys con
P2X0LI	PNP set P2xr[7:4]	PNPRDP, A79	LDN=0,279=61	rd-wr	sys con
P2X6HI	PNP set P2xr[9:8]	PNPRDP, A79	LDN=0,279=62	rd-wr	sys con
P2X6LI	PNP set P2xr[7:4]	PNPRDP, A79	LDN=0,279=63	rd-wr	sys con
P2X8HI	PNP set P2xr[9:8]	PNPRDP, A79	LDN=0,279=64	rd-wr	sys con
P2X8LI	PNP set P2xr[7:4]	PNPRDP, A79	LDN=0,279=65	rd-wr	sys con
P3X0HI	PNP set P3xr[9:8]	PNPRDP, A79	LDN=0,279=66	rd-wr	sys con
P3X0LI	PNP set P3xr[7:4]	PNPRDP, A79	LDN=0,279=67	rd-wr	sys con
PHCAI	PNP set PCODAR[9:8]	PNPRDP, A79	LDN=0,279=68	rd-wr	sys con
PLCAI	PNP set PCODAR[7:2]	PNPRDP, A79	LDN=0,279=69	rd-wr	sys con

FIG. 10B

Mnemonic	Description	I/O Addr.	Index	Rd-Wr	Module
PUI1SI	PNP Audio IRQ Channel 1 Select	PNPRDP, A79	LDN=0,279=70	rd-wr	sys con
PUI1TI	PNP Audio IRQ Channel 1 Type	PNPRDP	LDN=0,279=71	read	sys con
PUI2SI	PNP Audio IRQ Channel 2 Select	PNPRDP, A79	LDN=0,279=72	rd-wr	sys con
PUI2TI	PNP Audio IRQ Channel 2 Type	PNPRDP	LDN=0,279=73	read	sys con
PUD1SI	PNP Audio DMA Channel 1 Select	PNPRDP, A79	LDN=0,279=74	rd-wr	sys con
PUD2SI	PNP Audio DMA Channel 2 Select	PNPRDP, A79	LDN=0,279=75	rd-wr	sys con
PSEENI	PNP Serial EEPROM Enable	PNPRDP, A79	LDN=0,279=F0	rd-wr	sys con
PSECI	PNP Serial EEPROM Control	PNPRDP, A79	LDN=0,279=F1	rd-wr	sys con
PPWRI	PNP Power Mode	PNPRDP, A79	LDN=0,279=F2	rd-wr	sys con
PRACTI	PNP CD-ROM Activate Register	PNPRDP, A79	LDN=1,279=30	rd-wr	sys con
PRRCI	PNP CD-ROM I/ORange Check Reg.	PNPRDP, A79	LDN=1,279=31	rd-wr	sys con
PRAHI	PNP set PCDRAR[9:8]	PNPRDP, A79	LDN=1,279=60	rd-wr	sys con
PRALI	PNP set PCDRAR[7:4]	PNPRDP, A79	LDN=1,279=61	rd-wr	sys con
PRISI	PNP CD-ROM IRQ Select	PNPRDP, A79	LDN=1,279=70	rd-wr	sys con
PRITI	PNP CD-ROM IRQ Type	PNPRDP	LDN=1,279=71	read	sys con
PRDSI	PNP CD-ROM DMA Select	PNPRDP, A79	LDN=1,279=74	rd-wr	sys con

FIG. 10C

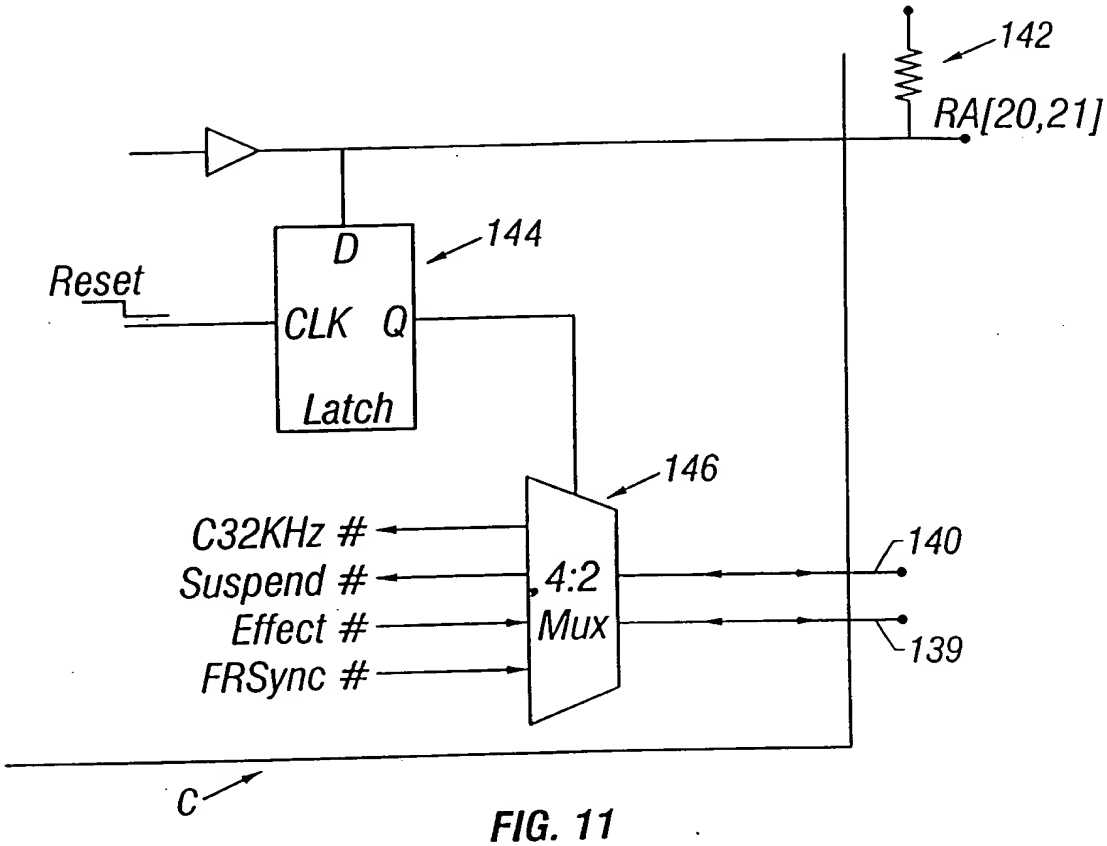

142
RA[20,21]
D
144
Reset
CLK Q
Latch
146
C32KHz #
Suspend #
Effect #
FRSync #
4:2
Mux
140
139
C

FIG. 11

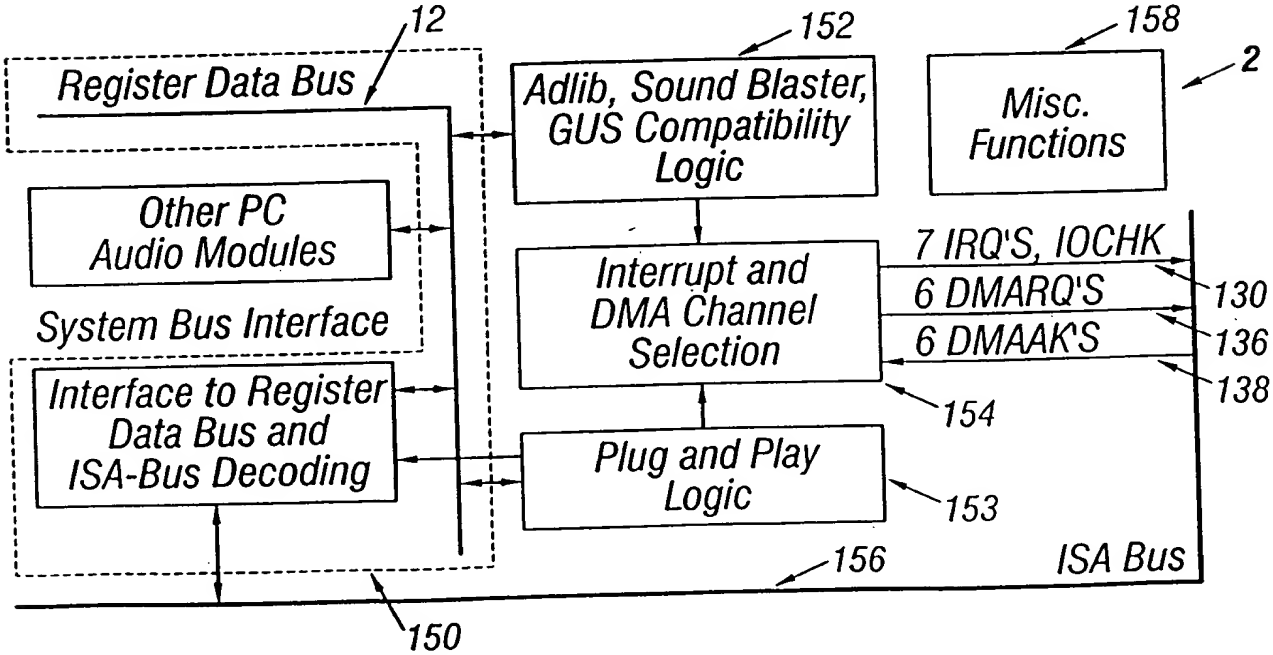

12
Register Data Bus
152
Adlib, Sound Blaster,
GUS Compatibility
Logic
158
Misc.
Functions
2
Other PC
Audio Modules
System Bus Interface
Interface to Register
Data Bus and
ISA-Bus Decoding
Interrupt and
DMA Channel
Selection
7 IRQ'S, IOCHK
6 DMARQ'S
6 DMAAK'S
130
136
138
154
Plug and Play
Logic
153
156
ISA Bus
150

FIG. 12

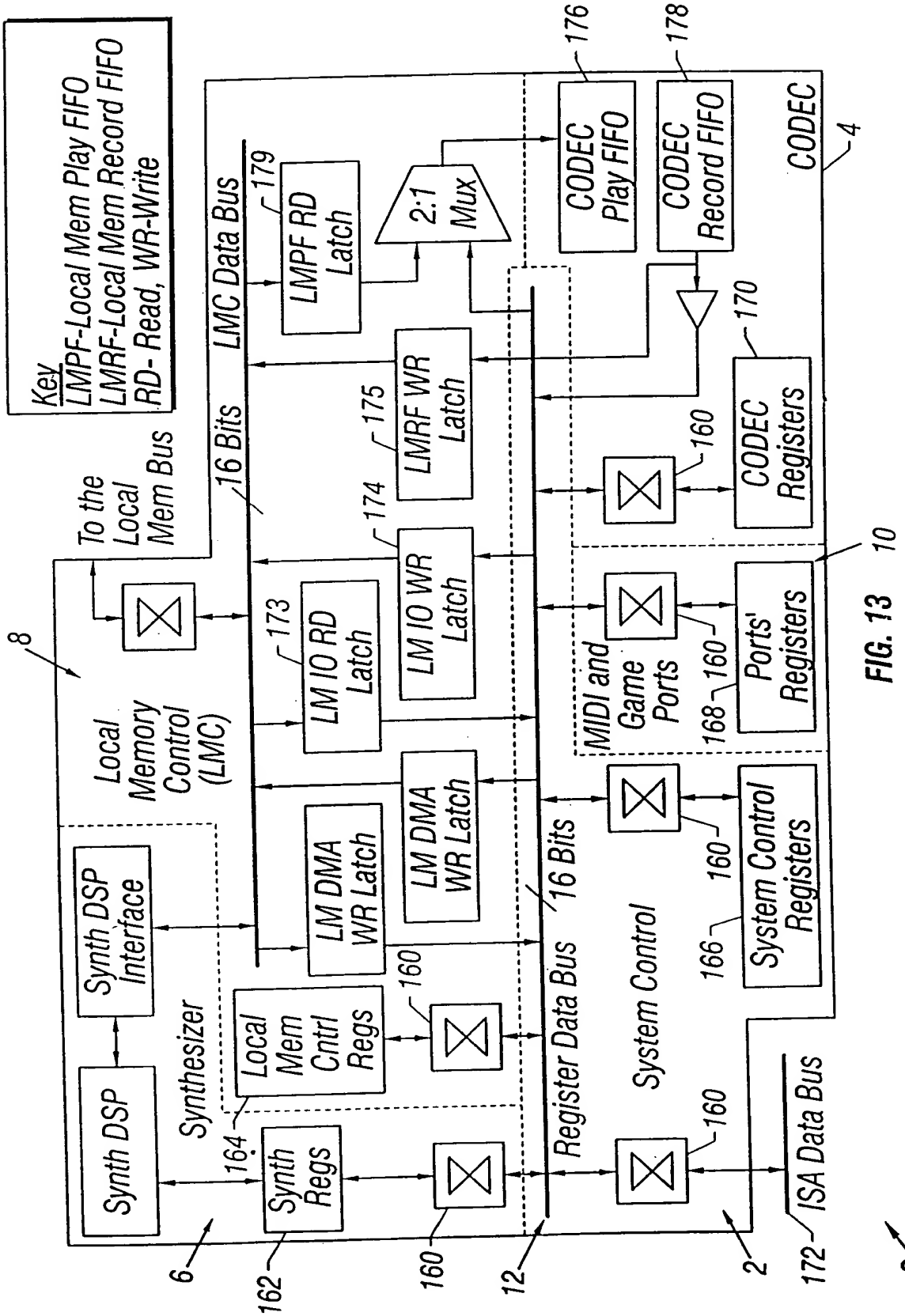

Key
LMPF-Local Mem Play FIFO
LMRF-Local Mem Record FIFO
RD- Read, WR-Write
To the Local Mem Bus
16 Bits
LMC Data Bus
Local Memory Control (LMC)
8
LMPF RD Latch
179
2:1 Mux
CODEC Play FIFO
176
CODEC Record FIFO
178
CODEC
4
LMRF WR Latch
175
170
CODEC Registers
160
LM IO RD Latch
173
LM IO WR Latch
174
MIDI and Game Ports
Ports' Registers
168
10
LM DMA WR Latch
LM DMA WR Latch
16 Bits
Register Data Bus
System Control
System Control Registers
166
Synth DSP Interface
Synthesizer
Local Mem Cntrl Regs
164
Synth DSP
Synth Regs
ISA Data Bus
6
162
12
2
172
C

FIG. 13

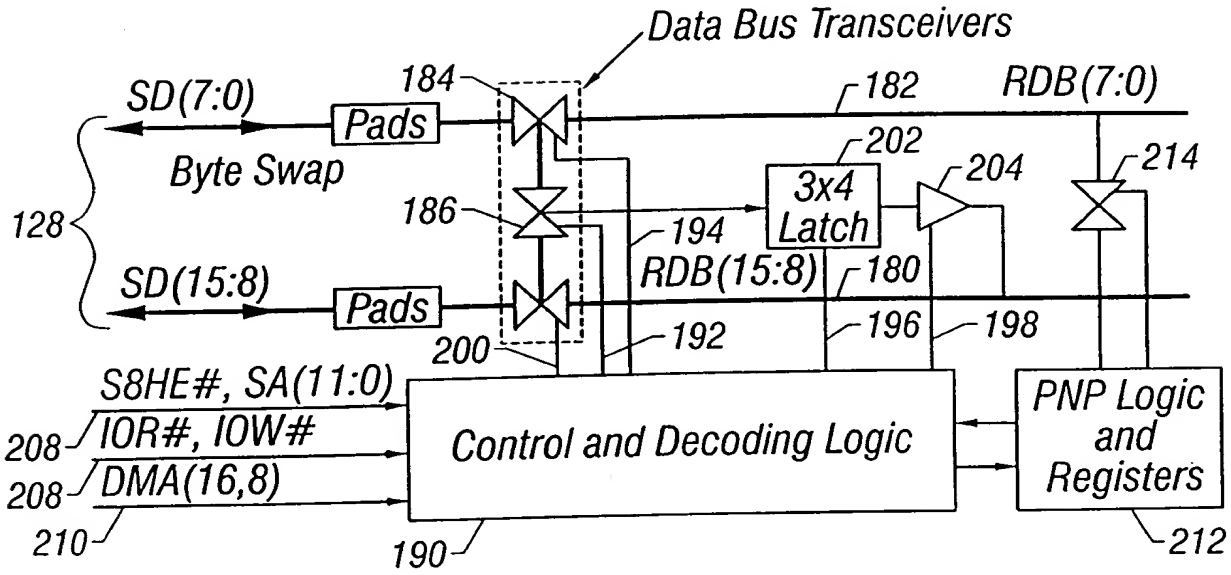


FIG. 14A

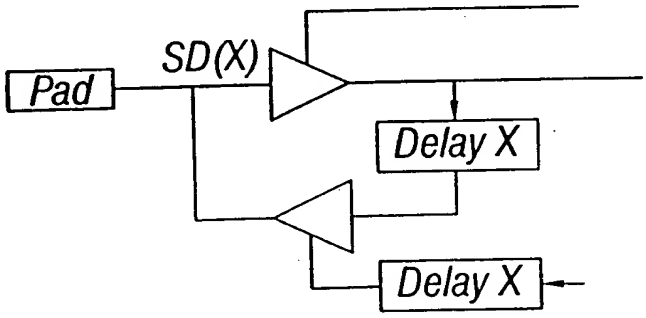


FIG. 14B

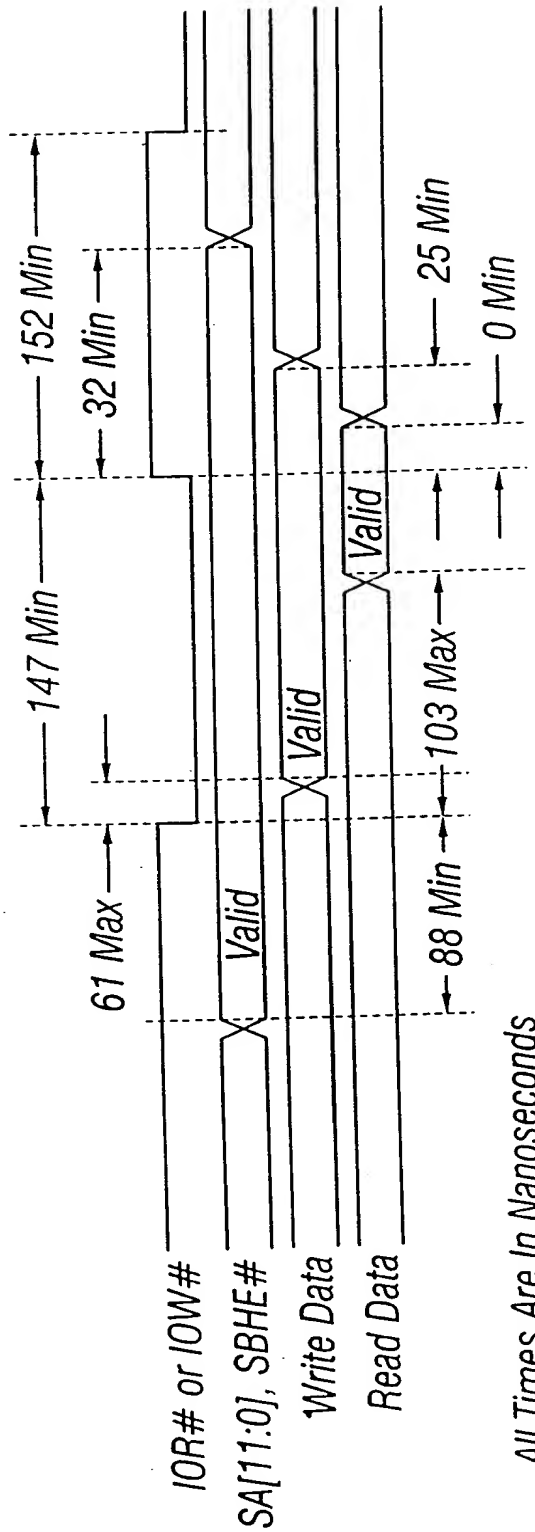


FIG. 15

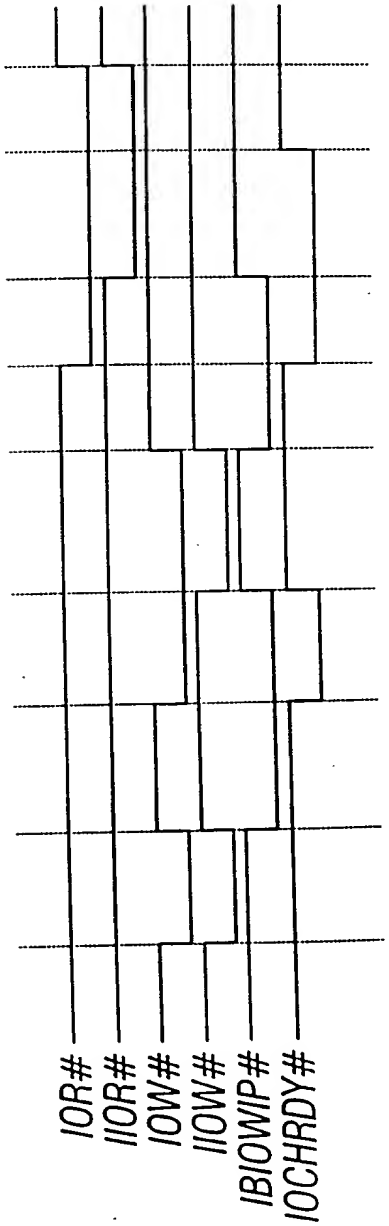


FIG. 16A

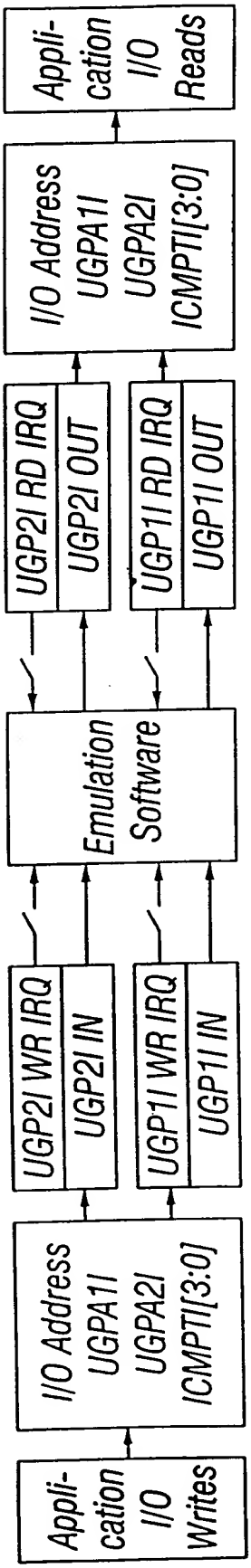

Appli-
cation
I/O
Writes
I/O Address
UGPA1I
UGPA2I
ICMPTI[3:0]
UGP2I WR IRQ
UGP2I IN
UGP1I WR IRQ
UGP1I IN
Emulation
Software
UGP2I RD IRQ
UGP2I OUT
UGP1I RD IRQ
UGP1I OUT
I/O Address
UGPA1I
UGPA2I
ICMPTI[3:0]
Appli-
cation
I/O
Reads

FIG. 16B

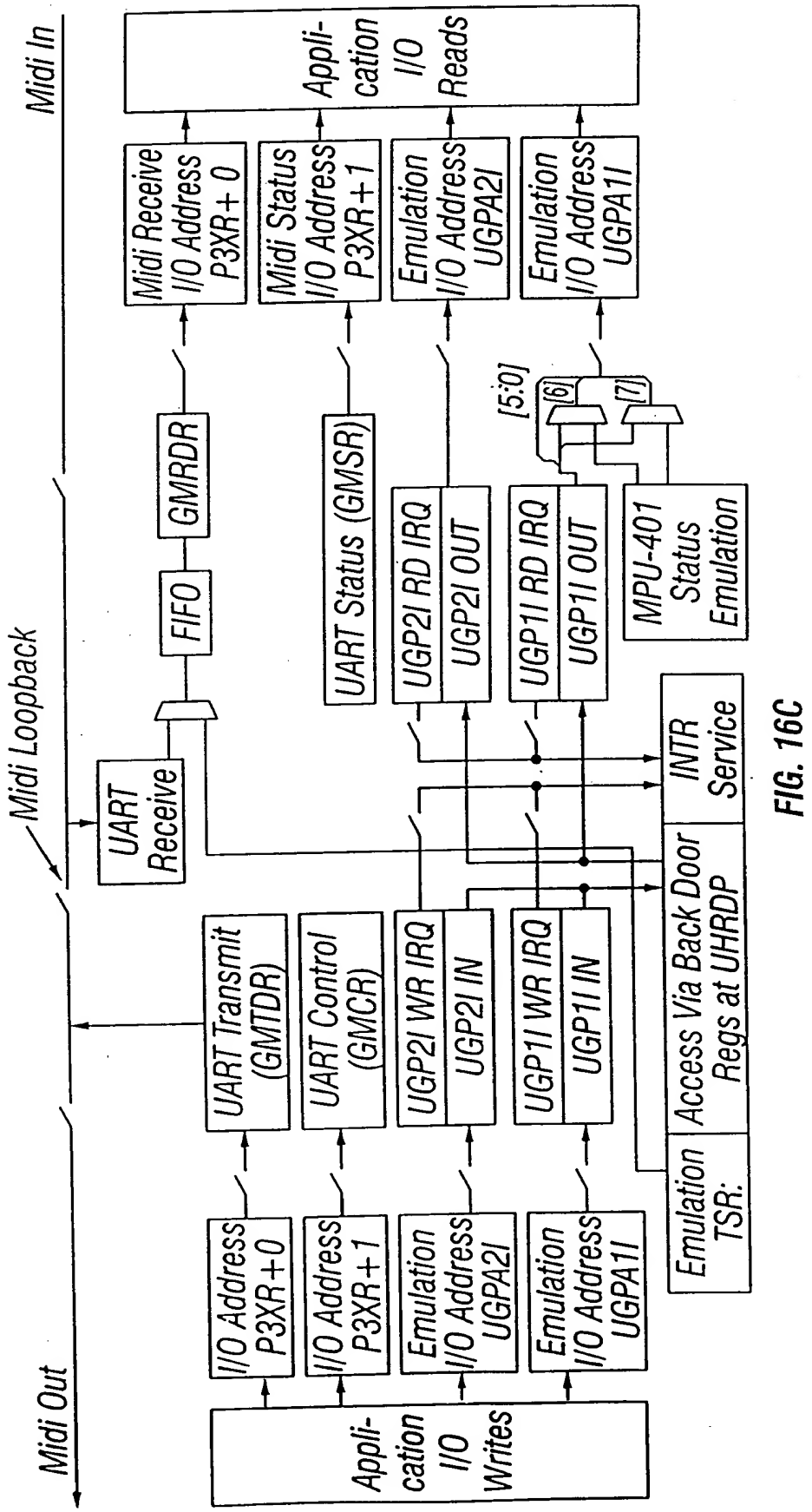

Midi In
Midi Loopback
Midi Out
Appli-cation I/O Reads
Midi Receive I/O Address P3XR+ 0
Midi Status I/O Address P3XR+ 1
Emulation I/O Address UGPA2I
Emulation I/O Address UGPA1I
GMRDR
FIFO
UART Receive
UART Status (GMSR)
UGP2I RD IRQ
UGP2I OUT
UGP1I RD IRQ
UGP1I OUT
[5:0]
[6]
[7]
MPU-401 Status Emulation
INTR Service
Access Via Back Door Regs at UHRDP
Emulation TSR:
UART Transmit (GMTDR)
UART Control (GMCR)
UGP2I WR IRQ
UGP2I IN
UGP1I WR IRQ
UGP1I IN
I/O Address P3XR+0
I/O Address P3XR+1
Emulation I/O Address UGPA2I
Emulation I/O Address UGPA1I
Appli-cation I/O Writes

FIG. 16C

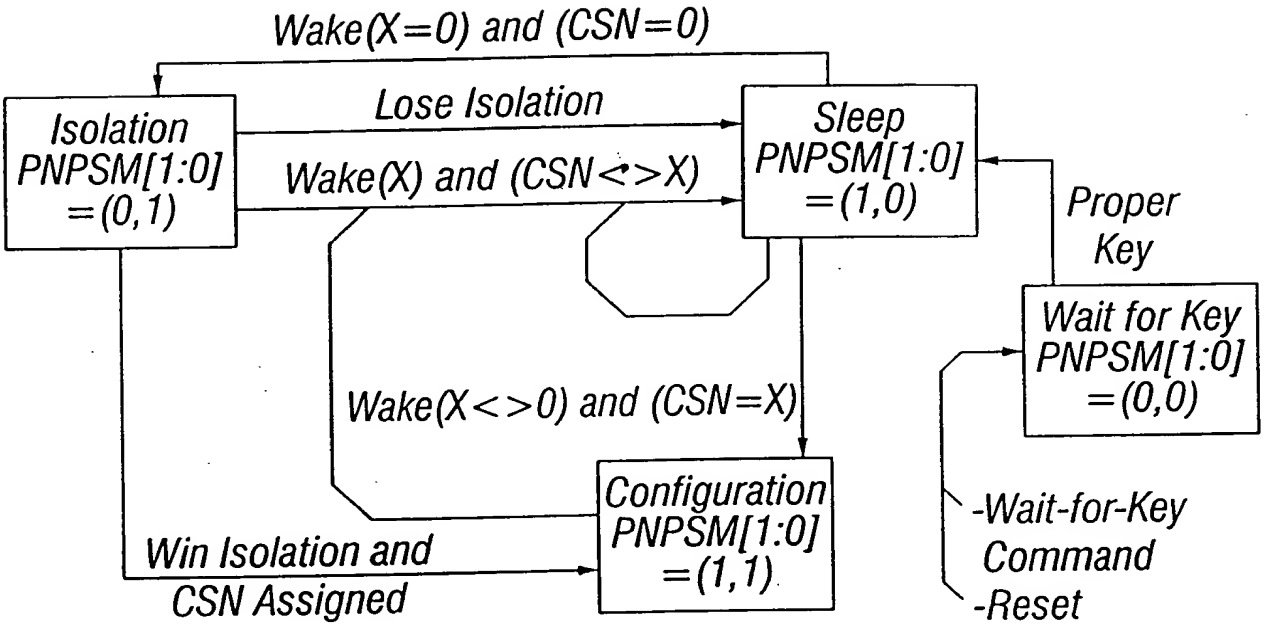

Wake(X=0) and (CSN=0)
Isolation
PNPSM[1:0]
=(0,1)
Lose Isolation
Wake(X) and (CSN<>X)
Sleep
PNPSM[1:0]
=(1,0)
Proper
Key
Wait for Key
PNPSM[1:0]
=(0,0)
Wake(X<>0) and (CSN=X)
Configuration
PNPSM[1:0]
=(1,1)
Win Isolation and
CSN Assigned
-Wait-for-Key
Command
-Reset

FIG. 17

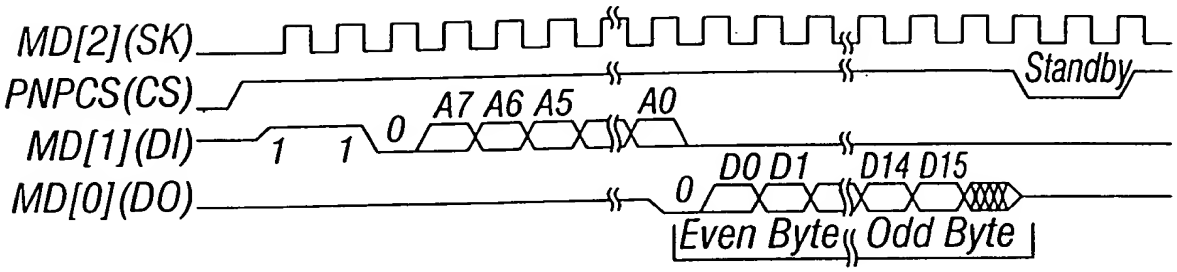


FIG. 18

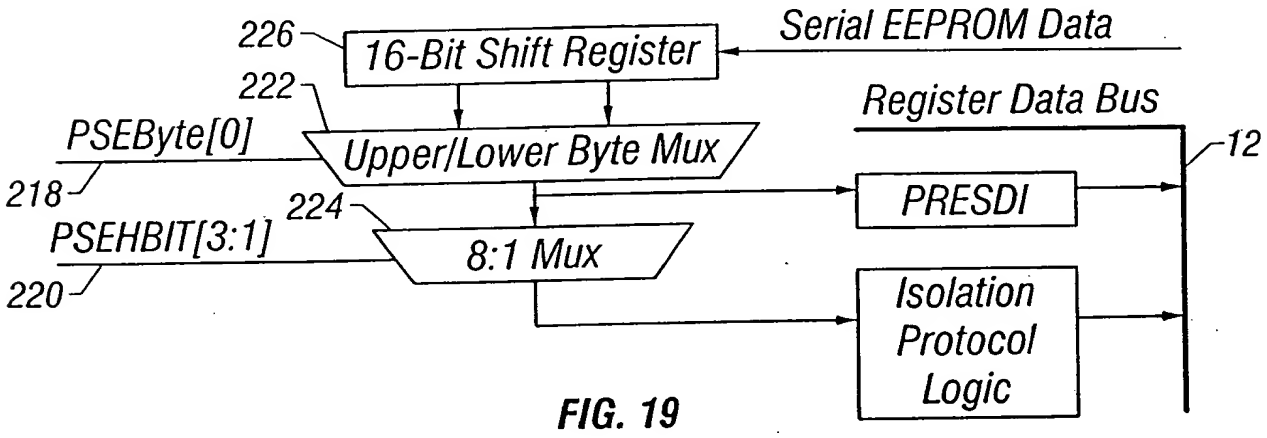


FIG. 19

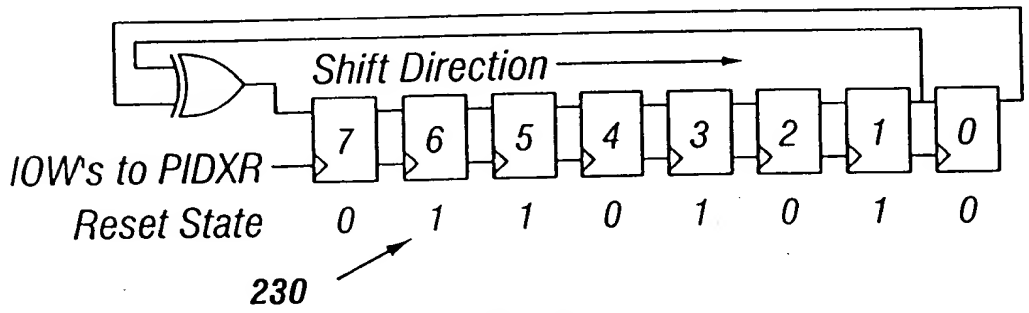


FIG. 20

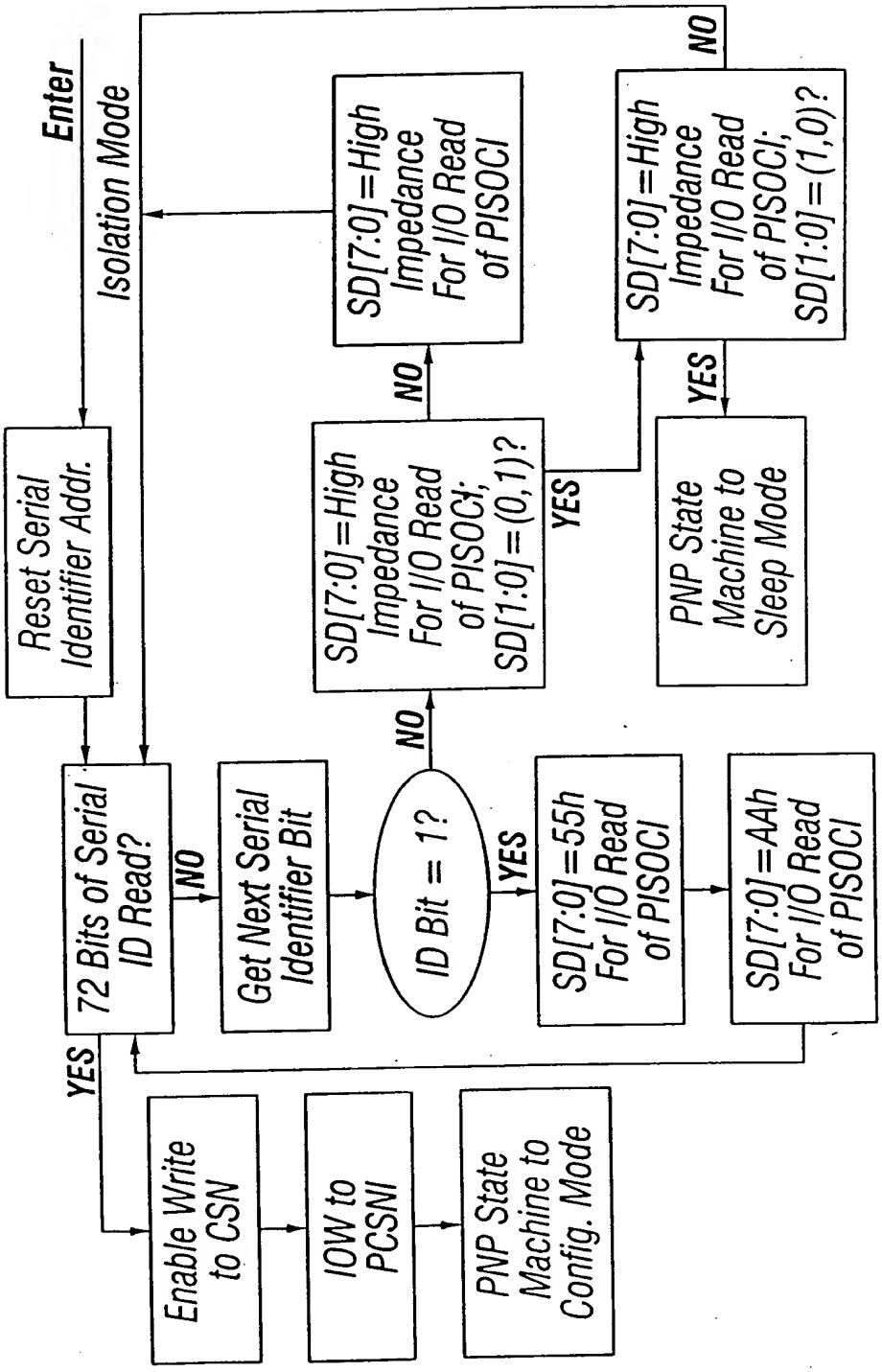

Enter Isolation Mode
Reset Serial Identifier Addr.
72 Bits of Serial ID Read?
NO
Get Next Serial Identifier Bit
ID Bit = 1?
NO
YES
SD[7:0]=55h For I/O Read of PISOCI
SD[7:0]=AAh For I/O Read of PISOCI
YES
Enable Write to CSN
IOW to PCSNI
PNP State Machine to Config. Mode
SD[7:0]=High Impedance For I/O Read of PISOCI; SD[1:0]=(0,1)?
NO
YES
SD[7:0]=High Impedance For I/O Read of PISOCI
PNP State Machine to Sleep Mode
SD[7:0]=High Impedance For I/O Read of PISOCI; SD[1:0]=(1,0)?
NO
YES

FIG. 21

Bytes	Description
9	header
3	plug and play version number
33	ANSI identifier string
6	AUDIO logical device
3	channel 1 IRQ allocation
3	channel 2 IRQ allocation
3	channel 1 DMA allocation
3	channel 2 DMA allocation
2	start dependent function priority 0
8	- I/O addr (min 220, max 220, length 1)
8	- I/O addr (min 226, max 226, length 1)
8	- I/O addr (min 228, max 228, length 8)
8	- I/O addr (min 320, max 320, length 8)
238	(repeat above dependent function 7 more times)
1	end dependent function
8	codec I/O address allocation (min 200, max 3FF,
	length 4, align 4)
4	joystick fixed I/O location (201, length 1)
4	AdLib fixed I/O location (388, length 2)
6	CD-ROM logical device
8	CD-ROM I/O address allocation (min 200, max 3FF,
	length 16, align 16)
3	CD-ROM IRQ allocation
3	CD-ROM DMA allocation
2	end tag
374	TOTAL

FIG. 22

Group	Event Description	IRQ Enables	Reporting Mechanism	Clear Mechanism
iasynth	synth voice reaches end of volume ramp	SVCI[5] & URSTI[2]	UISR[6], SVII[6], SVCI[7]	Set IGIDXR=8Fh
iasynth	synth voice finishes loop	SACI[5] & URSTI[2]	UISR[5], SVII[7], SVCI[7]	Set IGIDXR=8Fh
CIRQ	codec record sample counter rolls past zero	CFIG1I[1], mode 2 or 3	CSR3I[5], CSR1R[0]	IOW to CSR1R or CSR3I[5]=0
CIRQ	codec playback sample counter rolls past zero	CFIG1I[0]	CSR3I[4], CSR1R[0]	IOW to CSR1R or CSR3I[4]=0
CIRQ	codec record FIFO reaches threshold	CFIG3I[7], mode 3	CSR3I[5], CSR1R[0]	IOW to CSR1R or CSR3I[5]=0
CIRQ	codec playback FIFO reaches threshold	CFIG3I[6], mode 3	CSR3I[4], CSR1R[0]	IOW to CSR1R or CSR3I[4]=0
CIRQ	codec timer reaches zero	CFIG2I[6]	CSR3I[6], CSR1R[0]	IOW to CSR1R or CSR3I[6]=0
	extra IRQ: set enables	UDCI[7], UICI[6]	not reported	IOW to UDCI[7]=0
iaalsb	IOR of general port 1	URCR[6], URCR[3], IEMUBI[0]	USRR[4]	IOW to UCLRII
iaalsb	IOW to general port 1	URCR[6], URCR[3], IEMUBI[2]	USRR[3]	IOW to UCLRII

FIG. 23A

Group	Event Description	IRQ Enables	Reporting Mechanism	Clear Mechanism
iaalsb	IOR of general port 2	URCR[6], URCR[4], IEMUBI[1]	USRR[6]	IOW to UCLRII
iaalsb	IOW to general port 2	URCR[6], URCR[4], IEMUBI[3]	USRR[5]	IOW to UCLRII
iaalsb	IOR of 2xE	URCR[7]	USRR[7]	IOW to UCLRII
iasynth	TC (ISA bus) is reached for DMA to/from local memory (not the codec)	LDMACI[5]	UISR[7] & LDMACI[6]	IOR of LDMACI
iaalsb	IOW to AdLib data register (UADR)**	UASBCI[1]	UISR[4] & UASRR[0]	IOW of UASBCI[1]=0
iaalsb	IOW to SB U2x6R	UASBCI[5]	UISR[4] & UASRR[3]	IOW of UASBCI[5]=0
iaalsb	IOW to SB UI2XCR	UASBCI[5]	UISR[4] & UASRR[4]	IOW of UASBCI[5]=0
iaalsb	AdLib timer 1 rolls past FF	UASBCI[2]	UISR[2], UASRR[2]	IOW to UASBCI[2]=0
iaalsb	AdLib Timer 2 rolls past FF	UASBCI[3]	UISR[3], UASRR[1]	IOW to UASBCI[3]=0
iamidi	MIDI transmit ready	GMCR[6:5]	UISR[0]	IOW to GMTDR
iamidi	MIDI data received	GMCR[7]	UISR[1]	IOR of GMRDR
iacdrom	external function interrupt	PRACTI[0]	none	none

FIG. 23B

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

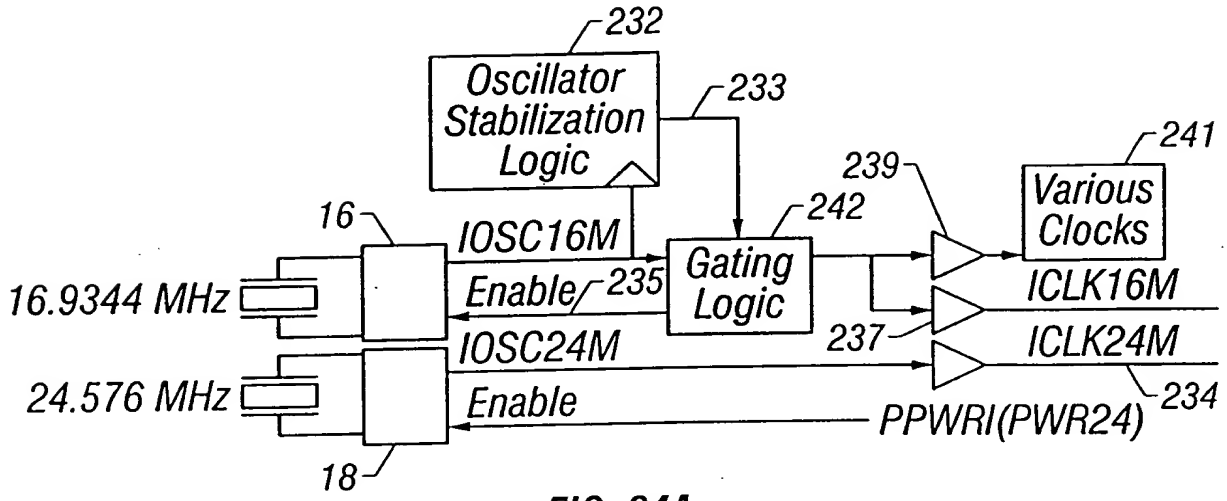


FIG. 24A

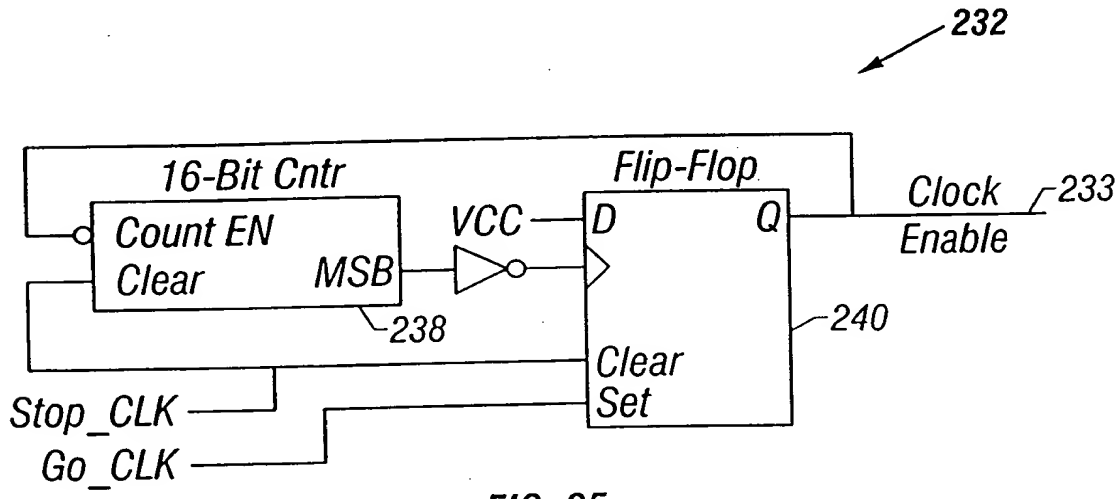


FIG. 25

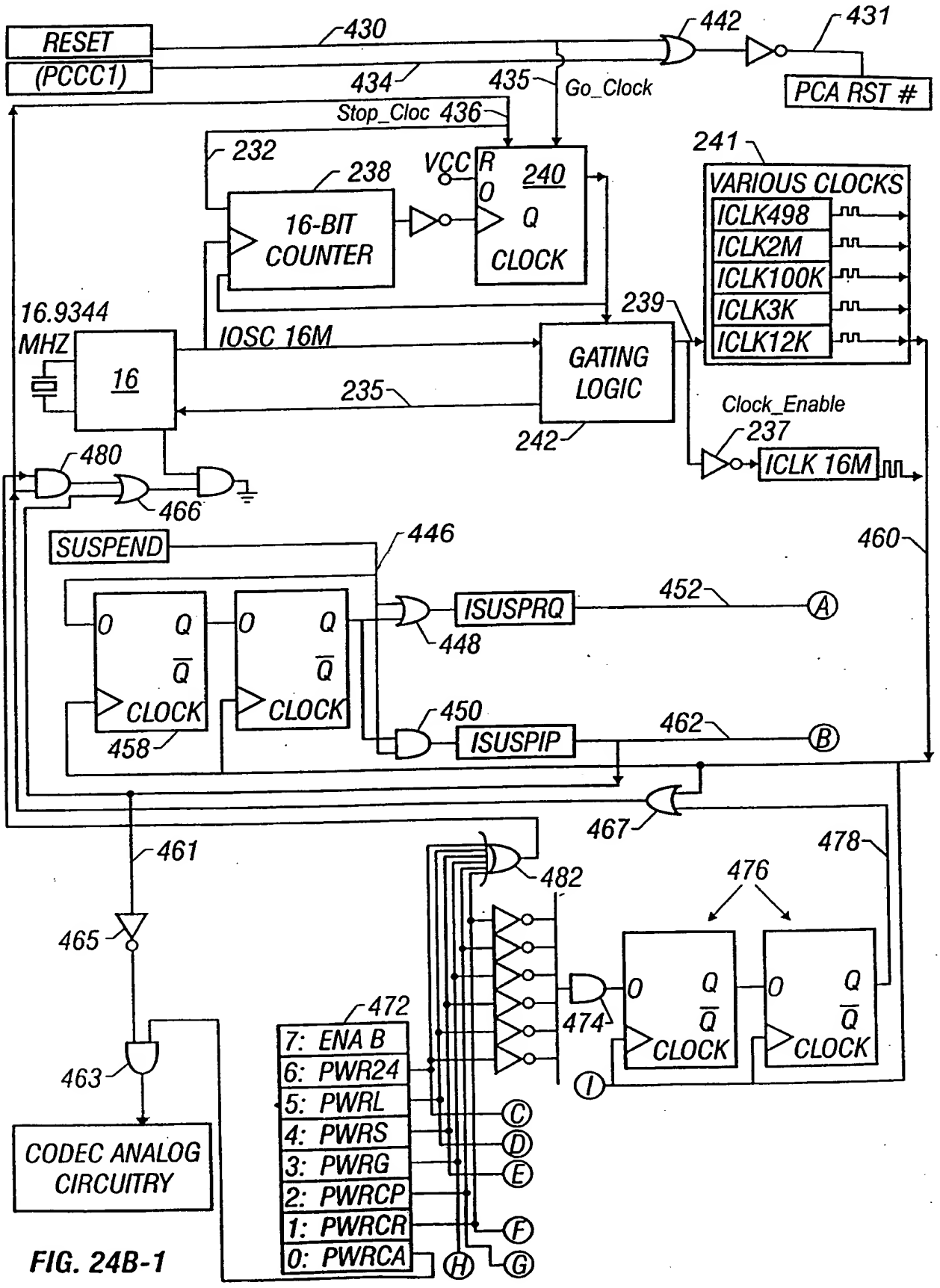

RESET
(PCCC1)
430
442
431
PCA RST #
434
435
Go_Clock
Stop_Cloc 436
232
238
VCC
R
240
16-BIT COUNTER
CLOCK
241
VARIOUS CLOCKS
ICLK498
ICLK2M
ICLK100K
ICLK3K
ICLK12K
16.9344 MHZ
16
IOSC 16M
239
GATING LOGIC
235
242
Clock_Enable
237
ICLK 16M
480
466
SUSPEND
446
460
452
ISUSPRQ
448
450
ISUSPIP
462
458
467
461
478
482
476
465
472
474
7: ENA B
6: PWR24
5: PWRL
4: PWRS
3: PWRG
2: PWRCP
1: PWRCR
0: PWRCA
463
CODEC ANALOG CIRCUITRY
A
B
C
D
E
F
G
H
I

FIG. 24B-1

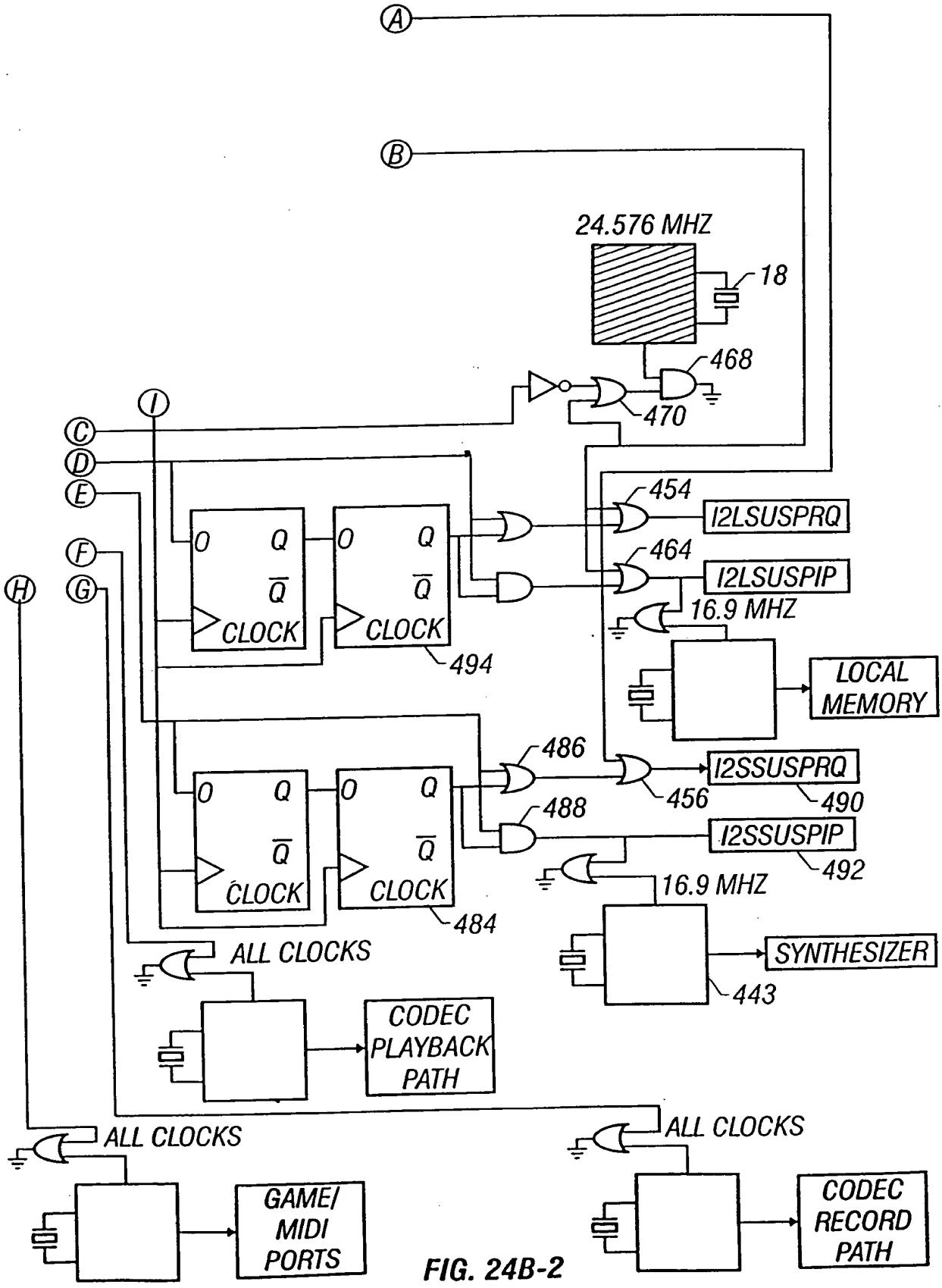

A
B
24.576 MHZ
18
468
470
I
C
D
E
F
G
H
454
I2LSUSPRQ
464
I2LSUSPIP
16.9 MHZ
LOCAL MEMORY
D Q
Q
CLOCK
494
486
I2SSUSPRQ
456
490
488
I2SSUSPIP
492
16.9 MHZ
484
ALL CLOCKS
SYNTHESIZER
443
CODEC PLAYBACK PATH
ALL CLOCKS
ALL CLOCKS
GAME/ MIDI PORTS
CODEC RECORD PATH

FIG. 24B-2

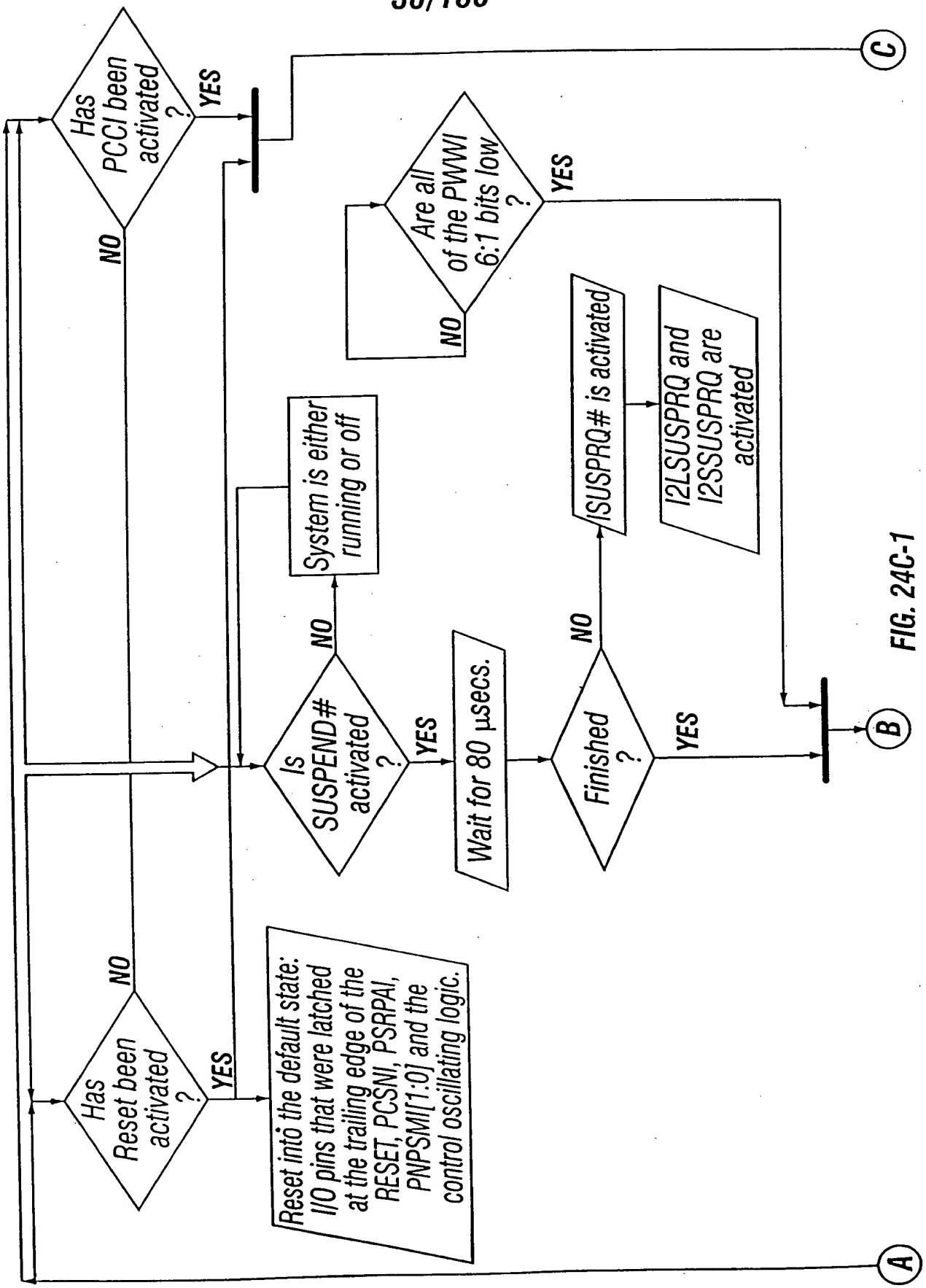

Has Reset been activated ?
NO
YES
Reset into the default state: I/O pins that were latched at the trailing edge of the RESET, PCSNI, PSRPAI, PNPSMI[1:0] and the control oscillating logic.
Has PCCI been activated ?
NO
YES
Is SUSPEND# activated ?
NO
YES
System is either running or off
Wait for 80 µsecs.
Finished ?
NO
YES
ISUSPRQ# is activated
I2LSUSPRQ and I2SSUSPRQ are activated
Are all of the PWWI 6:1 bits low ?
NO
YES
A
B
C

FIG. 24C-1

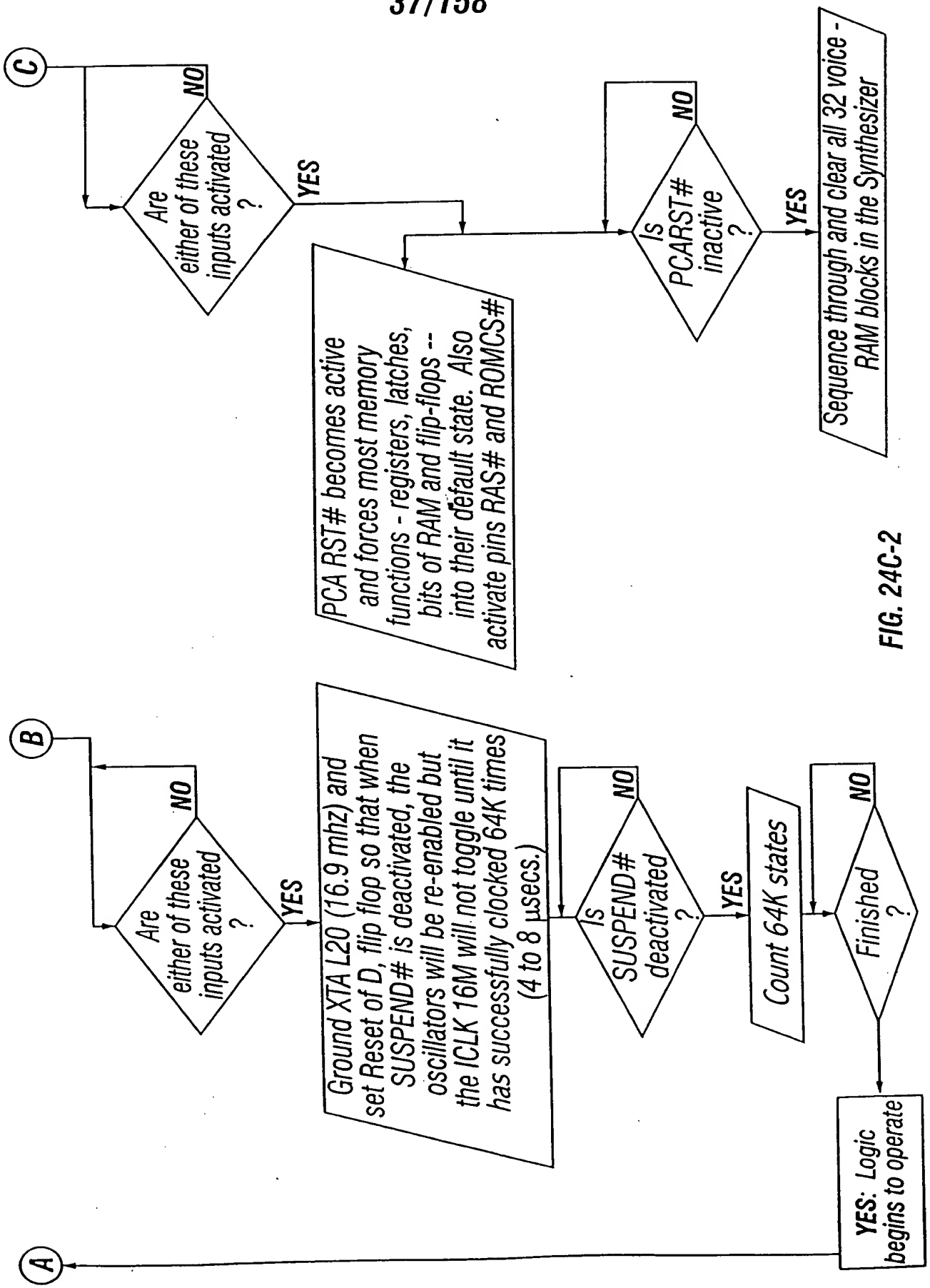

C
Are either of these inputs activated ?
NO
YES
PCA RST# becomes active and forces most memory functions - registers, latches, bits of RAM and flip-flops -- into their default state. Also activate pins RAS# and ROMCS#
Is PCARST# inactive ?
NO
YES
Sequence through and clear all 32 voice - RAM blocks in the Synthesizer
B
Are either of these inputs activated ?
NO
YES
Ground XTA L20 (16.9 mhz) and set Reset of D, flip flop so that when SUSPEND# is deactivated, the oscillators will be re-enabled but the ICLK 16M will not toggle until it has successfully clocked 64K times (4 to 8 µsecs.)
Is SUSPEND# deactivated ?
NO
YES
Count 64K states
Finished ?
NO
YES: Logic begins to operate
A

FIG. 24C-2

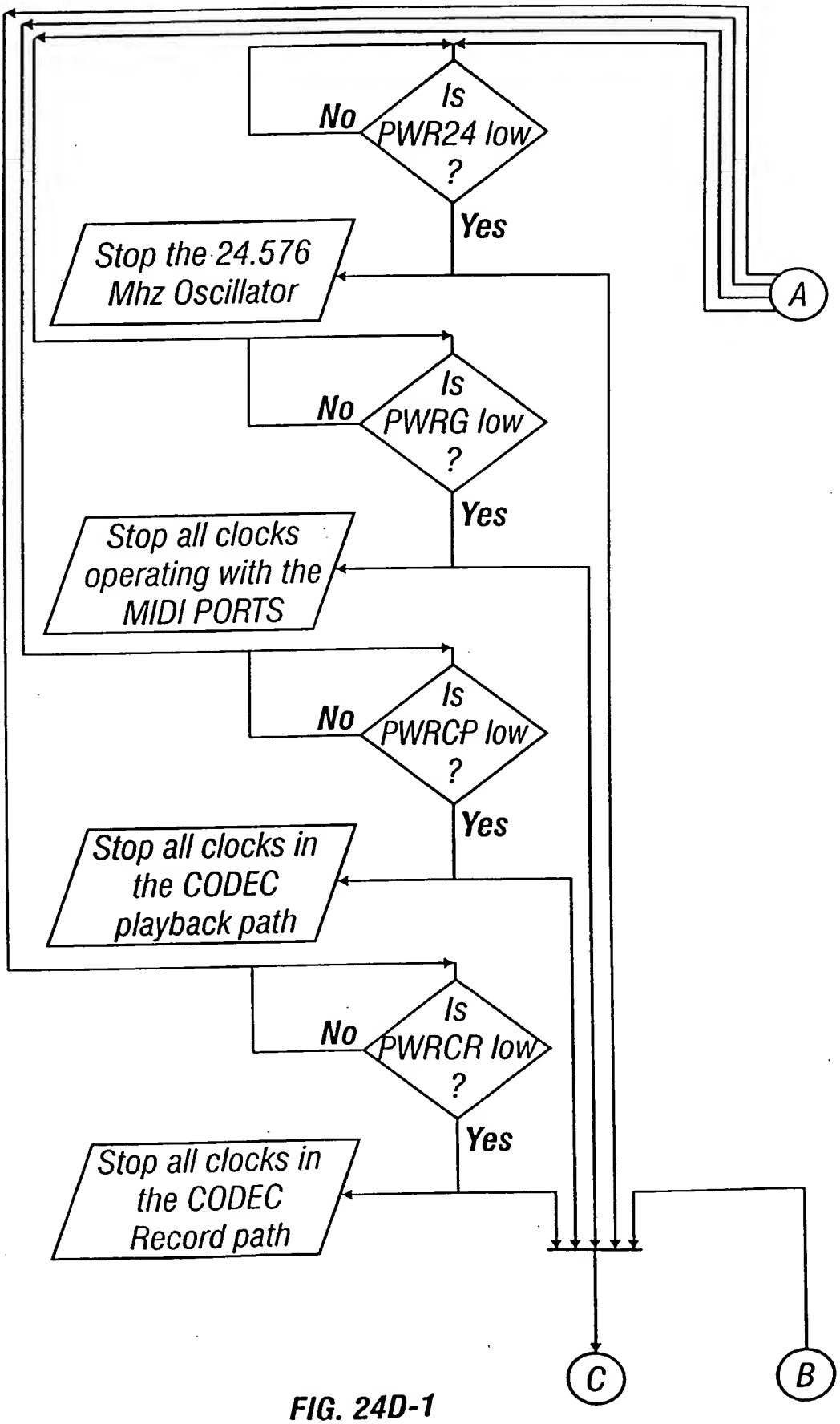

Is PWR24 low ?
No
Yes
Stop the 24.576 Mhz Oscillator
A
Is PWRG low ?
No
Yes
Stop all clocks operating with the MIDI PORTS
Is PWRCP low ?
No
Yes
Stop all clocks in the CODEC playback path
Is PWRCR low ?
No
Yes
Stop all clocks in the CODEC Record path
C
B

FIG. 24D-1

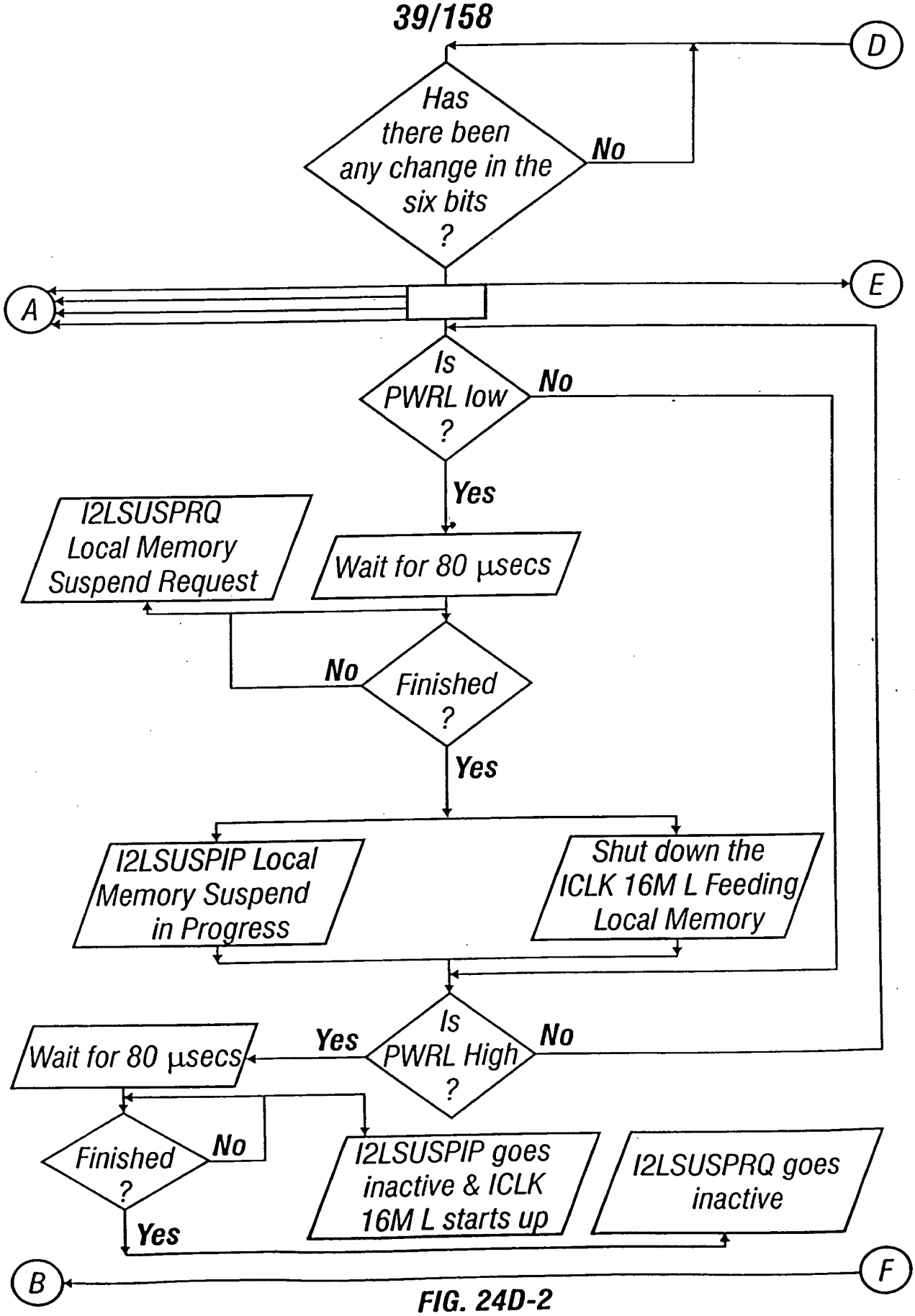

D
Has there been any change in the six bits ?
No
A
E
Is PWRL low ?
No
Yes
I2LSUSPRQ Local Memory Suspend Request
Wait for 80 µsecs
No
Finished ?
Yes
I2LSUSPIP Local Memory Suspend in Progress
Shut down the ICLK 16M L Feeding Local Memory
Is PWRL High ?
Yes
No
Wait for 80 µsecs
Finished ?
No
Yes
I2LSUSPIP goes inactive & ICLK 16M L starts up
I2LSUSPRQ goes inactive
B
F

FIG. 24D-2

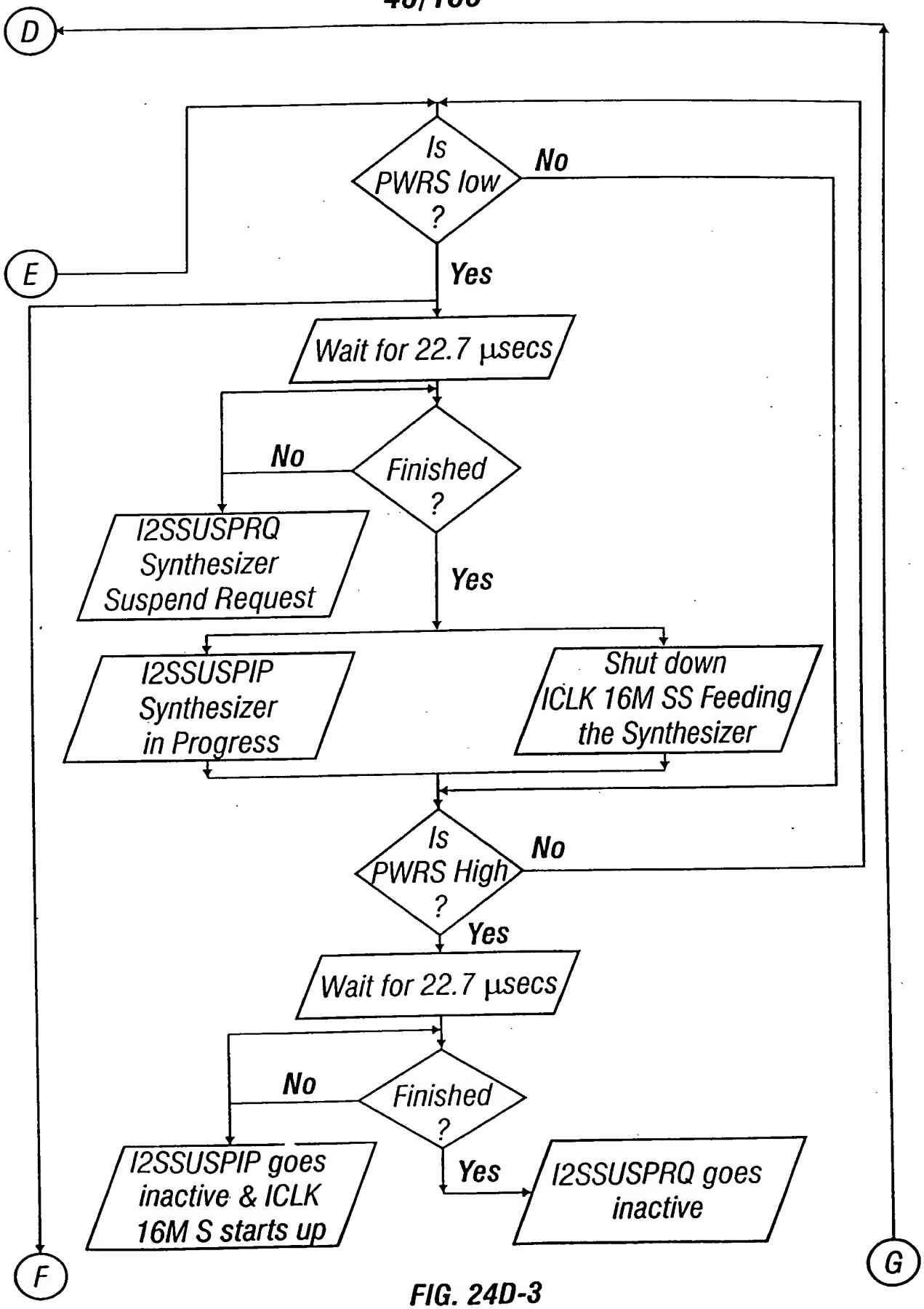

D
Is PWRS low ?
No
Yes
E
Wait for 22.7 μsecs
Finished ?
No
I2SSUSPRQ Synthesizer Suspend Request
Yes
I2SSUSPIP Synthesizer in Progress
Shut down ICLK 16M SS Feeding the Synthesizer
Is PWRS High ?
No
Yes
Wait for 22.7 μsecs
Finished ?
No
I2SSUSPIP goes inactive & ICLK 16M S starts up
Yes
I2SSUSPRQ goes inactive
F
G

FIG. 24D-3

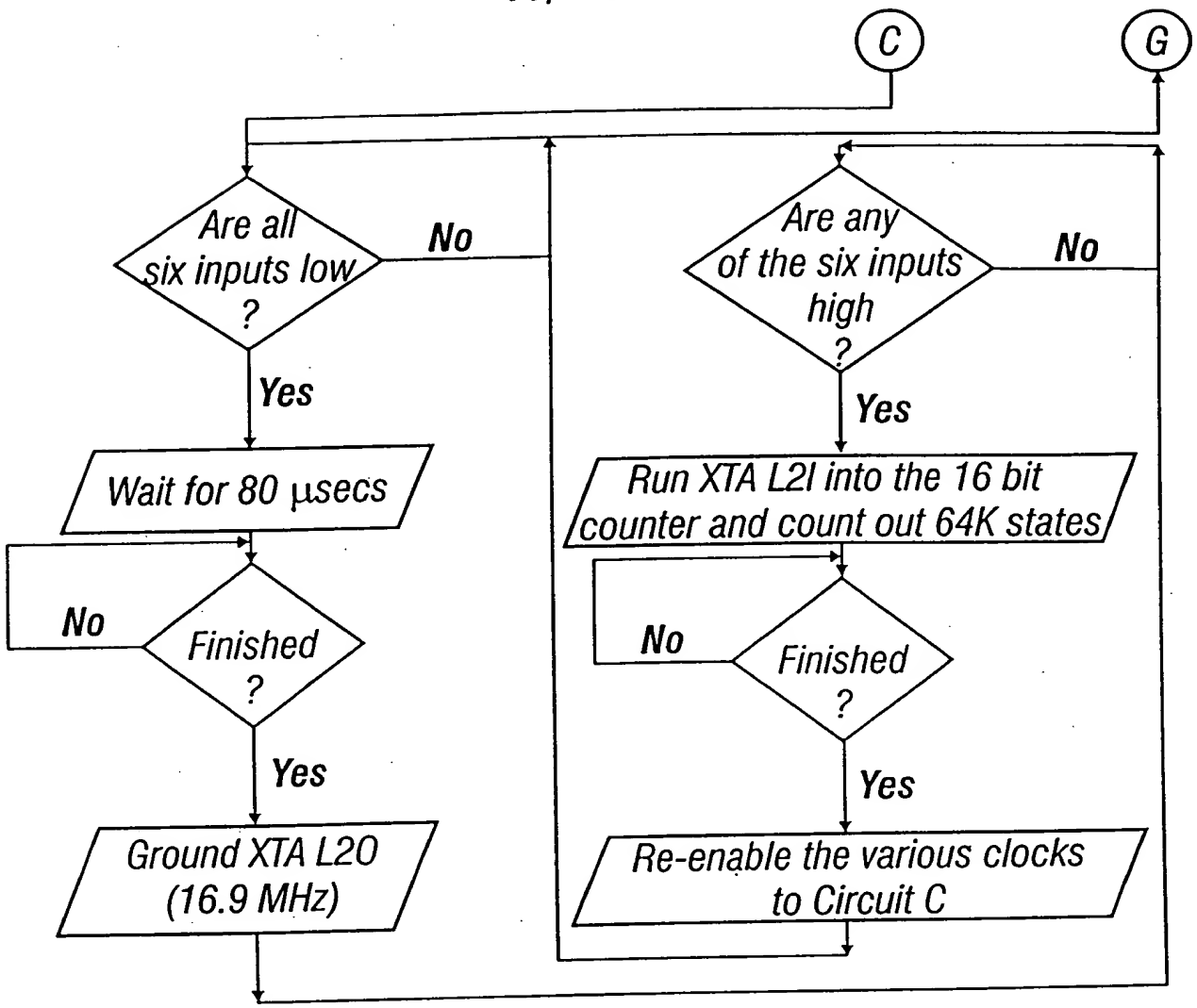

C
G
Are all six inputs low ?
No
Yes
Wait for 80 μsecs
No
Finished ?
Yes
Ground XTA L20 (16.9 MHz)
Are any of the six inputs high ?
No
Yes
Run XTA L2I into the 16 bit counter and count out 64K states
No
Finished ?
Yes
Re-enable the various clocks to Circuit C

FIG. 24D-4

PWR24, the 24.576 MHz. Oscillator from High to Low. I2C24SUSPRQ becomes active immediately and ICLK24M to the codec module is allowed to clock for at least 100 microseconds then turned off. It is stopped such that no glitches are possible; after a trailing edge, it stays low. After the clock is disabled the oscillator is disabled by grounding XTAL1O.
PWR24, the 24.576 MHz. Oscillator from Low to High. The oscillator is enabled and a 16-bit counter is allowed clock through 64K states to insure that the oscillator has stabilized. Then ICLK24M is allowed to start toggling without the possibility of glitching. At least 100 microseconds after that I2COSUSPRQ is disabled.
PWRL, Local Memory Control Enable from High to Low. I2LSUSPRQ becomes active immediately. ICLK16ML is allowed to toggle for at least 100 microseconds and then disabled without the possibility of glitching. After ICLK16ML stops toggling, I2LSUSPIP becomes active.
PWRL, Local Memory Control Enable from Low to High. I2LSUSPIP goes inactive immediately and ICLK16ML is allowed to start toggling without the possibility of glitching. At least 100 microseconds after that, I2LSUSPRQ goes inactive.

FIG. 26A

PWRS, Synth Enable from High to Low. I2SSUSPRQ becomes active immediately. ICLK16MS is allowed to toggle for at least 100 microseconds and then disabled without the possibility of glitching.
PWRS, Synth Enable from Low to High. ICLK16ML is immediately allowed to start toggling without the possibility of glitching. At least 100 microseconds after that, I2SSUSPRQ goes inactive.
PPWRI[3:0]. The state of these latches is driven off to their respective modules (bit[3] to the ports module and bits[2:0] to the codec module) to disable clocks and place circuitry in low-power mode.
Enter Shut-Down Mode. When PPWRI[6:1] are all cleared with a single I/O write, then, besides the activity to the individual modules described above, the 16.9 MHz. oscillator will be disabled. This is accomplished by waiting for at least 100 microseconds and then turning aff all clocks without possibility of glitching. Then the oscillator is disabled by grounding XTAL20.
Exit Shut-Down Mode. When any of the PPWRI[6:1] bits are set, then, besides the activity of the individual bits described above, the 16.9 MHz. oscillator will be re-enabled. First, the oscillator is re-enabled. XTAL I is run into a 16-bit counter to count our 64K states before it is assumed to be stable. At this point, the 16.9 MHz. clocks to various modules are allowed to start toggling without possibility of glitching. After the clocks start toggling, the bits that have been re-enabled start their routine, as described above.

FIG. 26B

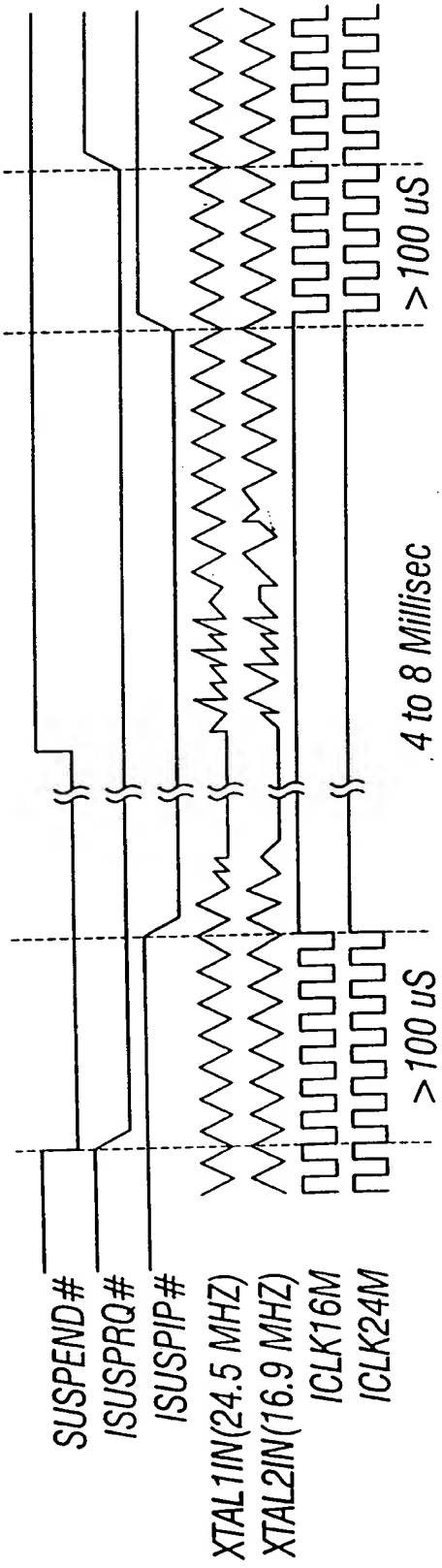

SUSPEND#
ISUSPRQ#
ISUSPIP#
XTAL1IN(24.5 MHZ)
XTAL2IN(16.9 MHZ)
ICLK16M
ICLK24M
>100 uS
4 to 8 Millisec
>100 uS

FIG. 27

Name	Qty	Type	Description
AEN	1	input	Address enable from the ISA bus, used to distinguish between DMA and I/O cycles.
C32KHZ	1	input	32KHZ Clock. Suspend-mode refresh clock for local DRAM. This pin can also be used as an output for the LMC's EFFECT# (see PIN SUMMARY in the general description part of this document).
CD_CS	1	output	Chip select to the CD-ROM controller. This can also be used for the external serial port (see PIN SUMMARY in the general description).
CD_DAK#	1	output	DMA acknowlege to the CD-ROM controller. This can also be used for the external serial port (see PIN SUMMARY in the general description).
CD_DRQ	1	input	DMA request from CD-ROM controller. This can also be used for the external serial port (see PIN SUMMARY in the general description).
CD_IRQ	1	input	Interrupt request from CD-ROM controller. This can also be used for the external serial port (see PIN SUMMARY in the general description).

FIG. 28A

Name	Qty	Type	Description
DAK[7,6,5, 3,1,0]#	6	input	The selectable DMA acknowledge lines from the ISA bus. DAK 0, 1, and 3 are used for 8-bit DMA transfers and DAK 5, 6, and 7 are used for 16-bit DMA.
DRQ[7,6,5, 3,1,0]#	6	oc output	The selectable DMA request lines to the ISA bus. DRQ 0, 1, and 3 are used for 8-bit DMA transfers and DRQ 5, 6, and 7 are used for 16-bit DMA.
IOCHRDY	1	oc output	I/O channel ready to the ISA bus, used to generate wait states.
IOCS16#	1	oc output	16-bit capability indication to the ISA bus.
IOR#	1	input	I/O read command from the ISA bus.
IOW#	1	input	I/O write command from the ISA bus.
IRQ[15,12,11, 7,5,3,2]	7	oc output	The selectable interrupt requests to the ISA bus.
IOCHK#	1	oc output	I/O channel check on the ISA bus; used to generate an NMI.
PNPCS	1	bi-dir	Active high output used as chip select for the Plug and Play serial EPROM. This is an input during reset; its state is latched by the trailing edge of RESET to determine if the IC is in PNP-compliant mode (low) or PNP-system mode (high).

FIG. 28B

Name	Qty	Type	Description
RESET	1	input	Reset from the ISA bus.
SA[11:0]	12	input	The 12 lower bits of the ISA address bus.
SBHE#	1	input	Byte high enable from the ISA address bus. When interfacing to an 8-bit ISA bus, this pin must be disconnected.
SD[15:0]	16	bi-dir	ISA data bus.
SUSPEND#	1	input	Low-power suspend mode. When active, all chip activity becomes frozen, the oscillators are turned off, C32KHZ is used to refresh DRAM, and most of the ISA-bus inputs and outputs are isolated from the IC. This pin can also be used as an output for the LMC's FRSYNC# (see PIN SUMMARY in the general description part of this document).
TC	1	input	Terminal Count indicates the end of a DMA group from the ISA bus.
XTAL1I	1	input	Crystal 1 input. Input from the 24.576 MHz. crystal.
XTAL1O	1	output	Crystal 1 ouput. Output to the 24.576 MHz. crystal.
XTAL2I	1	input	Crystal 2 input. Input from the 16.9344 MHz. crystal.
XTAL2O	1	output	Crystal 2 output. Output to the 16.9344 MHz. crystal.

FIG. 28C

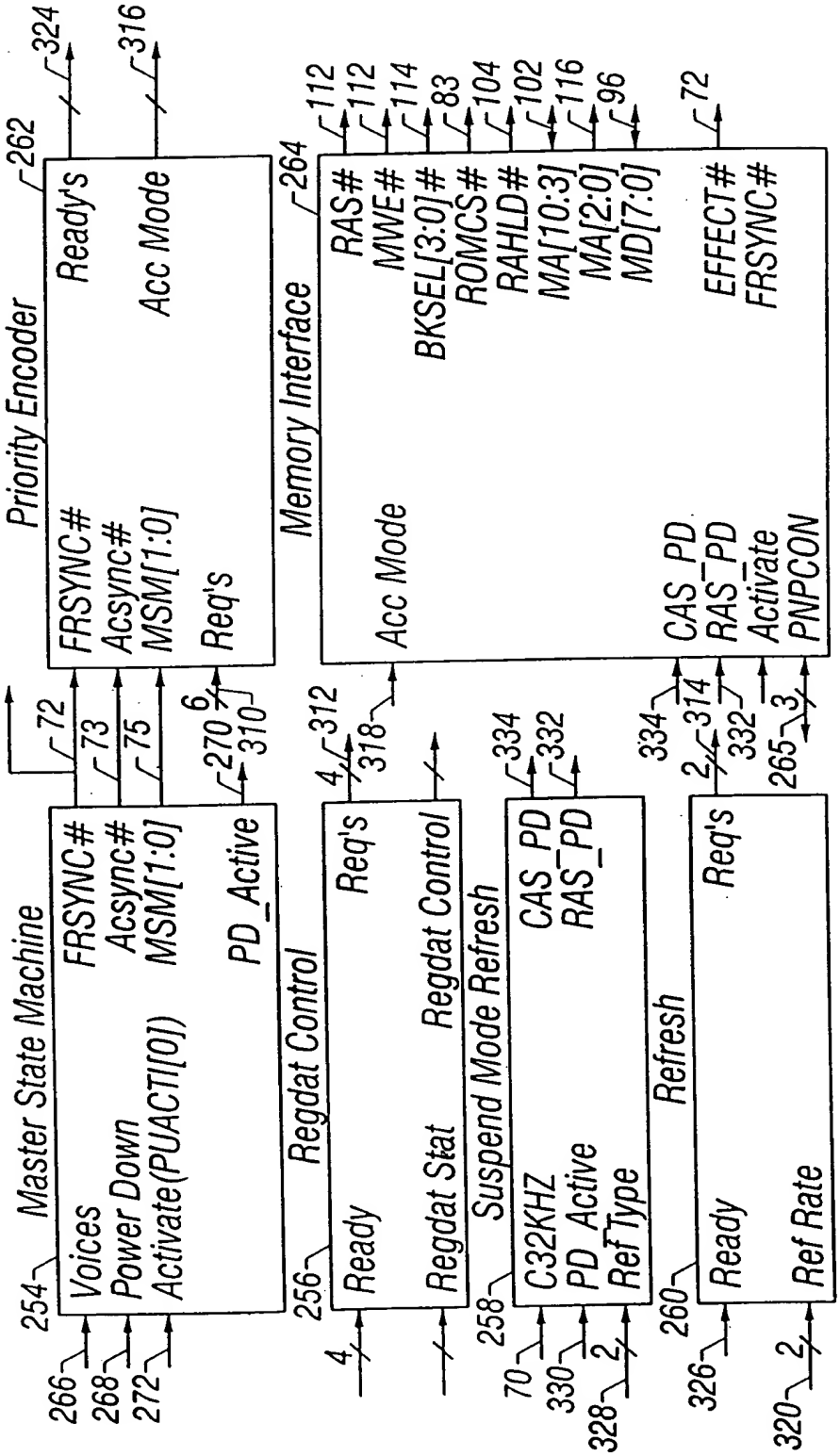

Master State Machine
254
Voices
Power Down
Activate(PUACTI[0])
FRSYNC#
Acsync#
MSM[1:0]
PD_Active
266
268
272
72
73
75
270
6
310
Priority Encoder
262
FRSYNC#
Acsync#
MSM[1:0]
Req's
Ready's
Acc Mode
324
316
Regdat Control
256
Ready
Req's
Regdat Stat
Regdat Control
4
312
318
Memory Interface
264
Acc Mode
RAS#
MWE#
BKSEL[3:0]#
ROMCS#
RAHLD#
MA[10:3]
MA[2:0]
MD[7:0]
CAS_PD
RAS_PD
Activate
PNPCON
EFFECT#
FRSYNC#
112
112
114
83
104
102
116
96
72
334
314
332
265
3
Suspend Mode Refresh
258
C32KHZ
PD_Active
RefType
CAS_PD
RAS_PD
70
330
328
2
334
332
Refresh
260
Ready
Req's
Ref Rate
326
320
2
2
8

FIG. 29

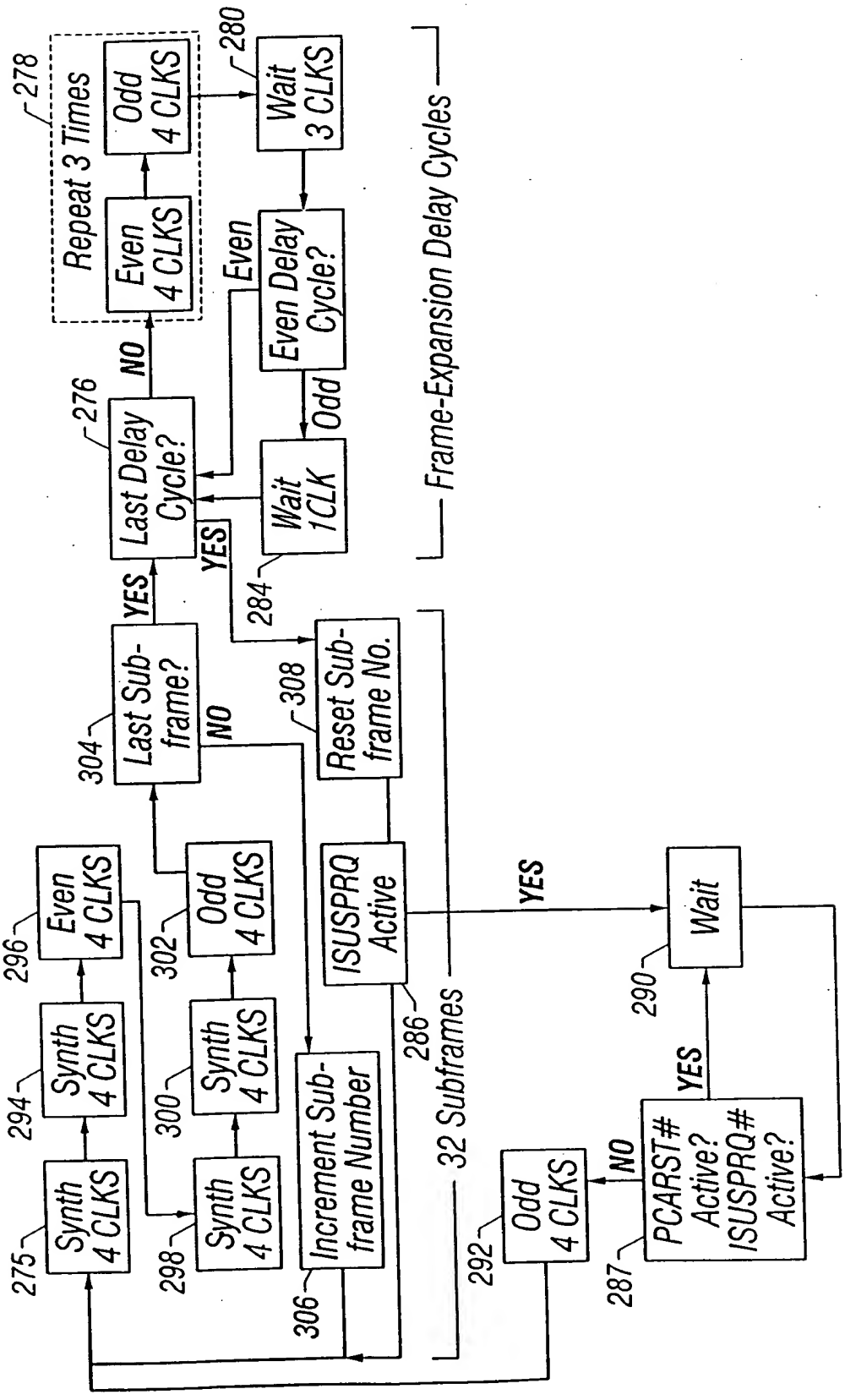

Synth 4 CLKS
275
Synth 4 CLKS
294
Even 4 CLKS
296
Synth 4 CLKS
298
Synth 4 CLKS
300
Odd 4 CLKS
302
Last Sub-frame?
304
YES
NO
Increment Sub-frame Number
306
Reset Sub-frame No.
308
ISUSPRQ Active
286
YES
32 Subframes
Frame-Expansion Delay Cycles
Odd 4 CLKS
292
NO
PCARST# Active? ISUSPRQ# Active?
287
YES
Wait
290
Repeat 3 Times
278
Even 4 CLKS
Odd 4 CLKS
Last Delay Cycle?
276
NO
YES
Even Delay Cycle?
Even
Odd
Wait 1CLK
284
Wait 3 CLKS
280

FIG. 30

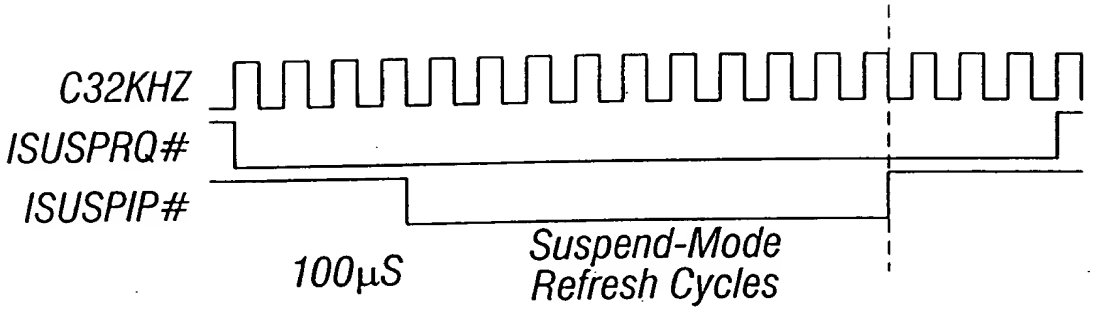


FIG. 31

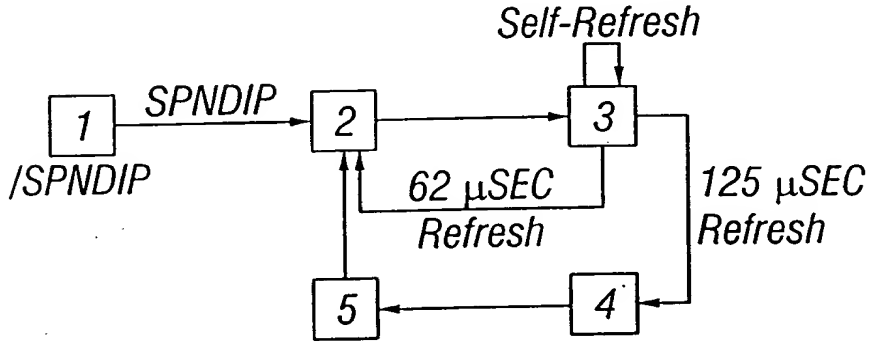


FIG. 32

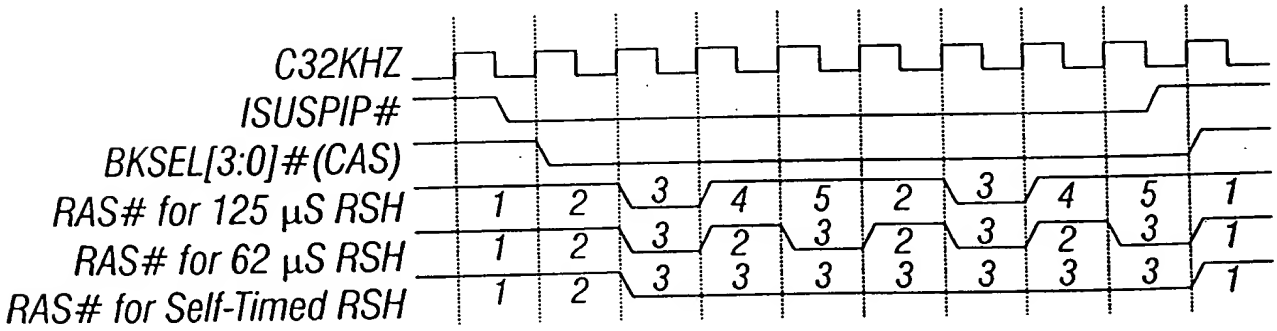


FIG. 33

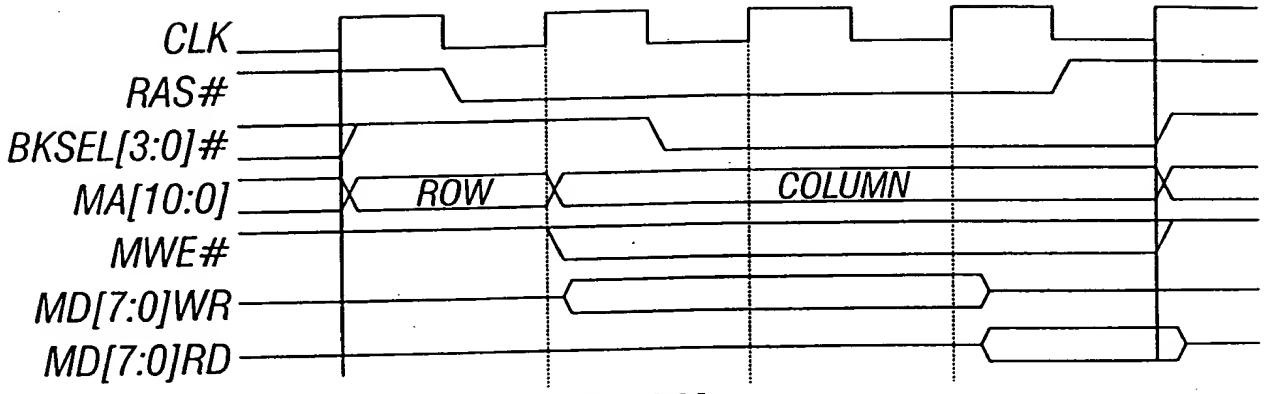


FIG. 34A

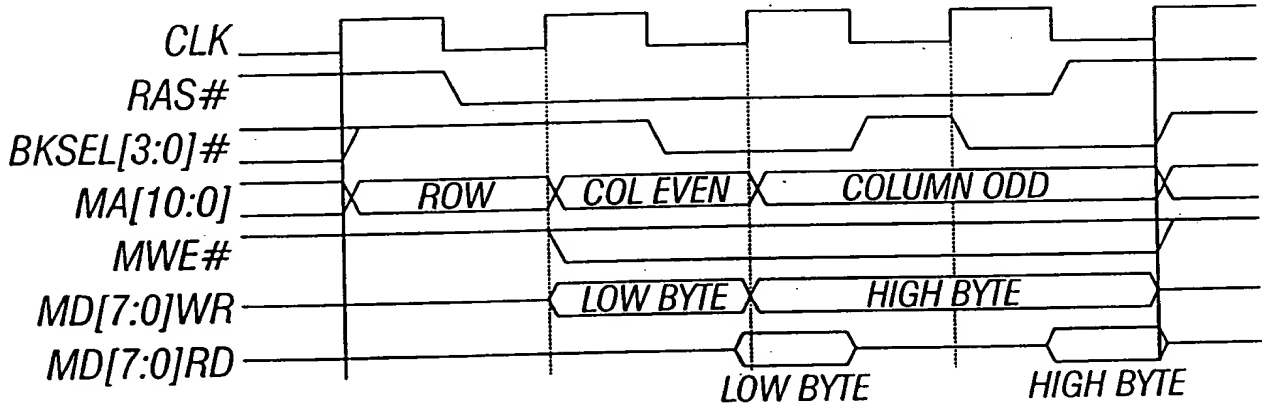


FIG. 34B

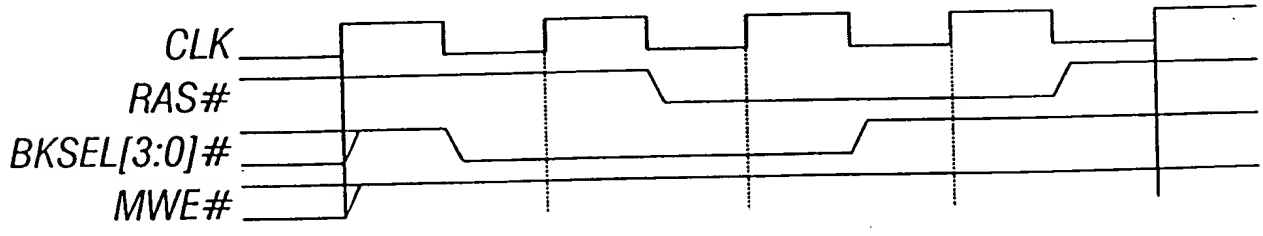


FIG. 34C

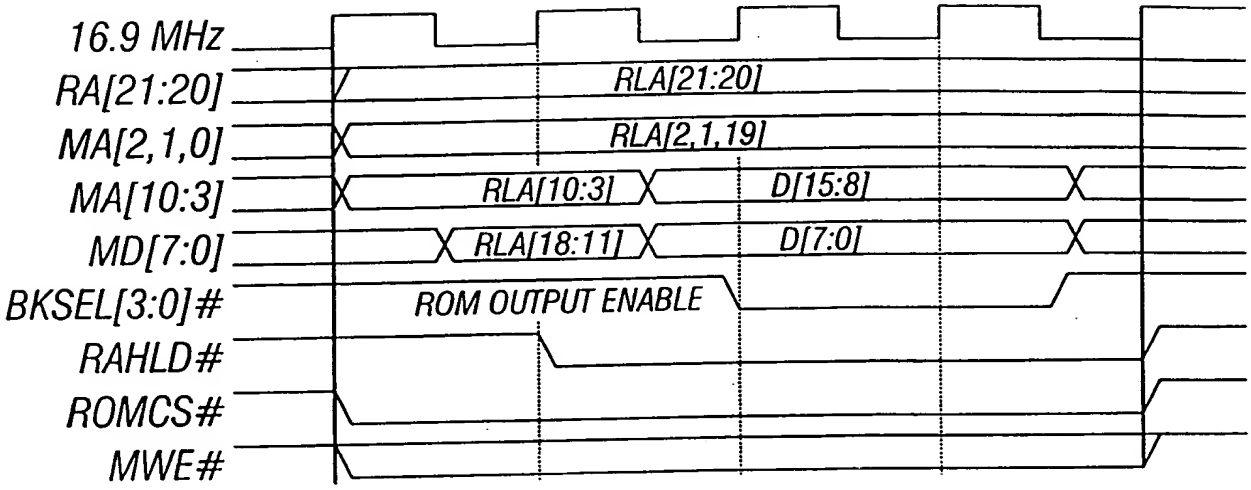

16.9 MHz
RA[21:20]
MA[2,1,0]
MA[10:3]
MD[7:0]
BKSEL[3:0]#
RAHLD#
ROMCS#
MWE#
RLA[21:20]
RLA[2,1,19]
RLA[10:3]
D[15:8]
RLA[18:11]
D[7:0]
ROM OUTPUT ENABLE

FIG. 35

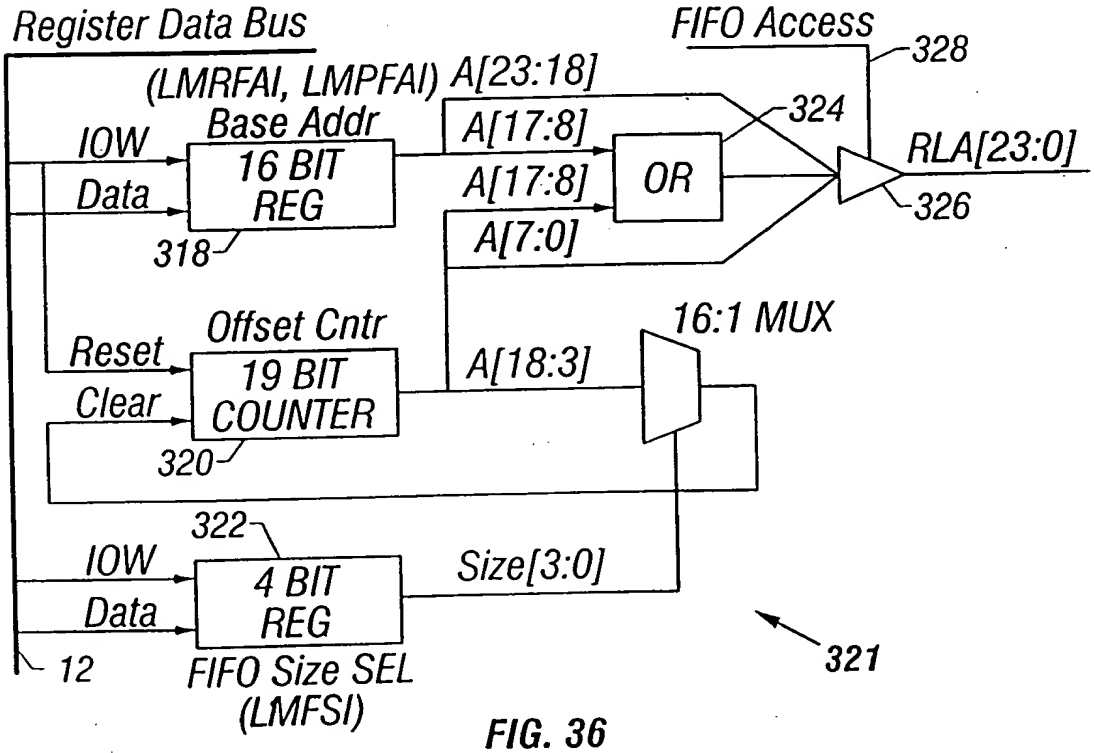

Register Data Bus
FIFO Access
328
(LMRFAI, LMPFAI) A[23:18]
Base Addr
IOW
Data
16 BIT
REG
318
A[17:8]
A[17:8]
A[7:0]
OR
324
RLA[23:0]
326
Offset Cntr
Reset
Clear
19 BIT
COUNTER
320
A[18:3]
16:1 MUX
322
IOW
Data
4 BIT
REG
Size[3:0]
12
FIFO Size SEL
(LMFSI)
321

FIG. 36

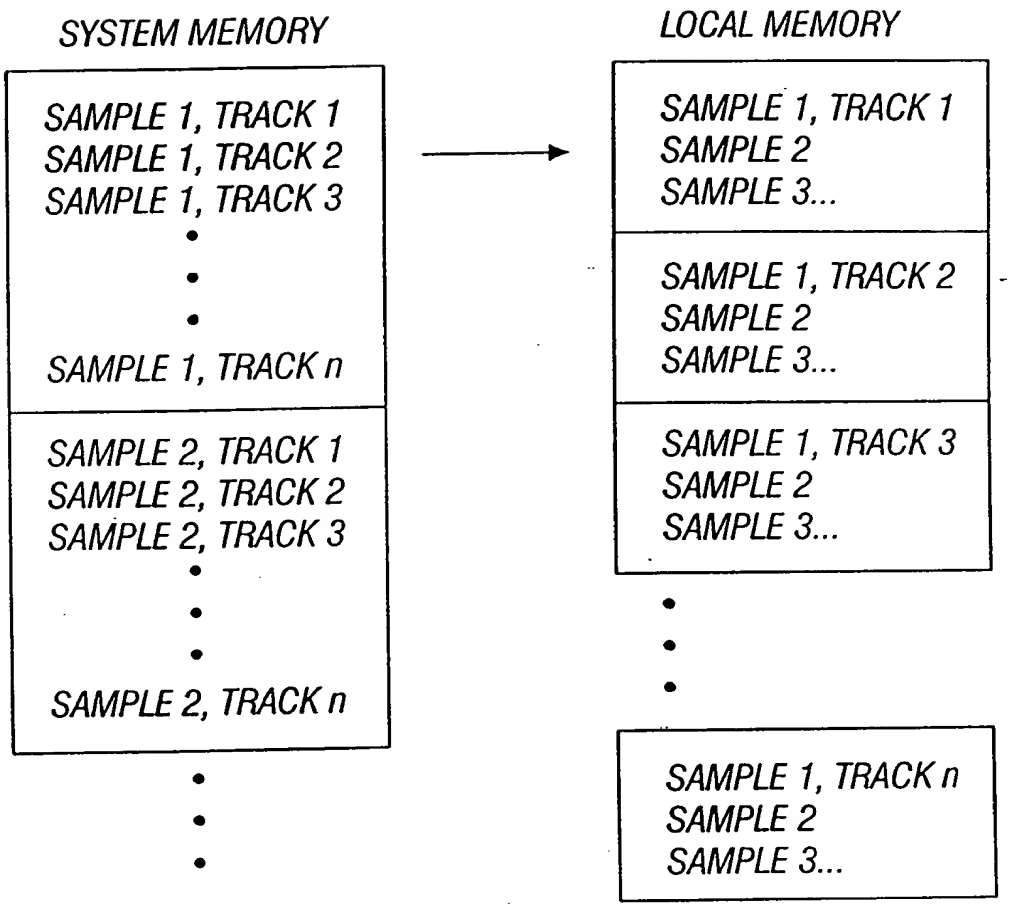

SYSTEM MEMORY
SAMPLE 1, TRACK 1
SAMPLE 1, TRACK 2
SAMPLE 1, TRACK 3
SAMPLE 1, TRACK n
SAMPLE 2, TRACK 1
SAMPLE 2, TRACK 2
SAMPLE 2, TRACK 3
SAMPLE 2, TRACK n
LOCAL MEMORY
SAMPLE 1, TRACK 1
SAMPLE 2
SAMPLE 3...
SAMPLE 1, TRACK 2
SAMPLE 2
SAMPLE 3...
SAMPLE 1, TRACK 3
SAMPLE 2
SAMPLE 3...
SAMPLE 1, TRACK n
SAMPLE 2
SAMPLE 3...

FIG. 37

DMA Chan	Sample Size	Description
8-bit	8-bit	Each DMA request-acknowledge cycle transfers one byte that is placed in the current track number; the track number increments with each byte transferred.
8-bit	16-bit	Each DMA request-acknowledge cycle transfers two bytes that are placed at the current track number; the track number increments with each 16-bit value transferred.
16-bit	8-bit	Each DMA request-acknowledge cycle transfers two bytes; the lower byte is placed in the current track number, the track number is incremented and the upper byte is placed in that track; the track number is then incremented again.
16-bit	16-bit	Each DMA request-acknowledge cycle transfers one 16-bit value that is placed in the current track number; the track number increments with each 16-bit value transferred.

FIG. 38

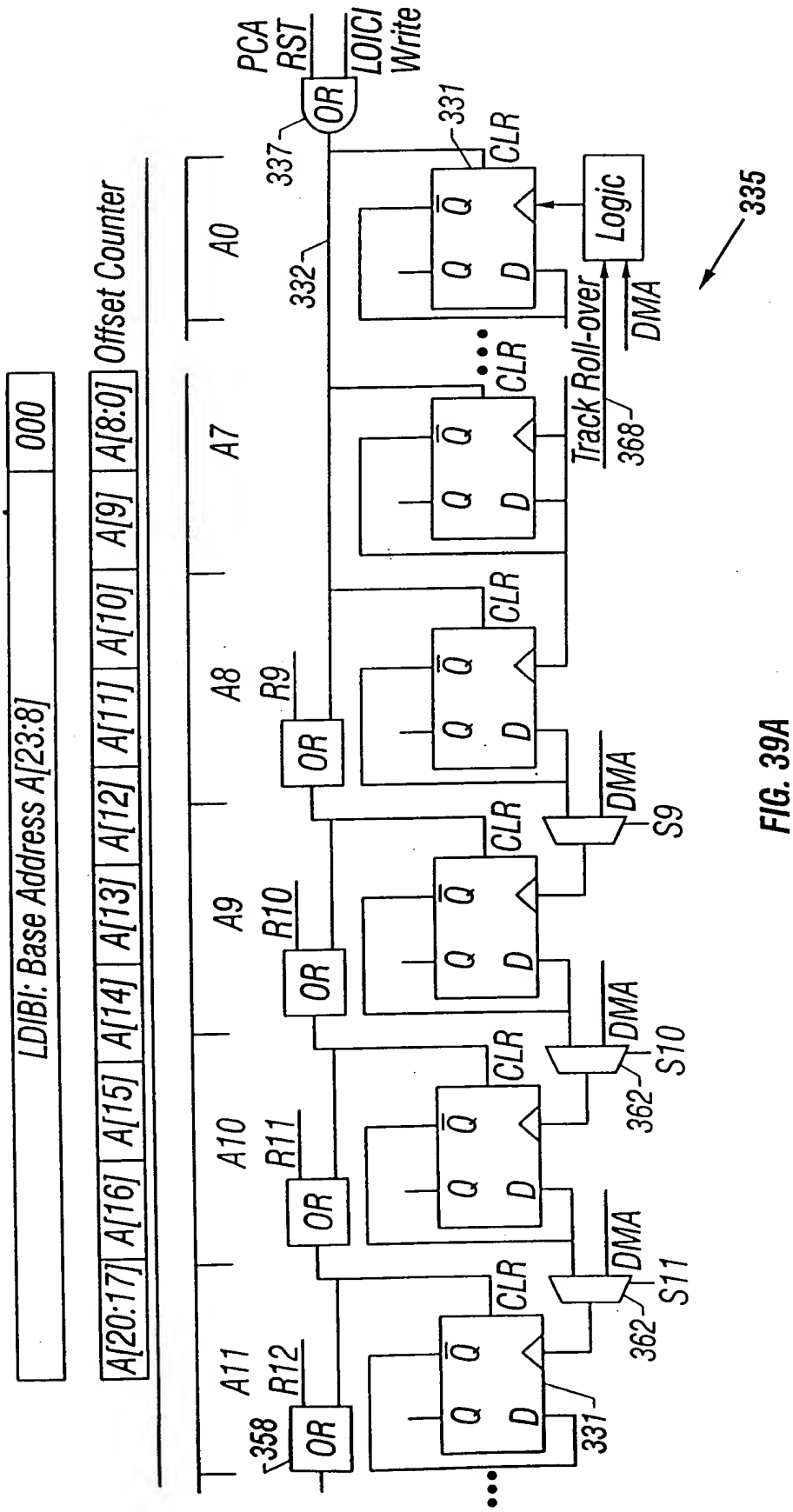

LDIBI: Base Address A[23:8]
000
A[20:17]
A[16]
A[15]
A[14]
A[13]
A[12]
A[11]
A[10]
A[9]
A[8:0]
Offset Counter
A11
A10
A9
A8
A7
A0
R12
R11
R10
R9
OR
358
337
332
PCA
RST
LOIC
Write
331
CLR
Q
D
Logic
335
Track Roll-over
368
DMA
S9
S10
S11
362

FIG. 39A

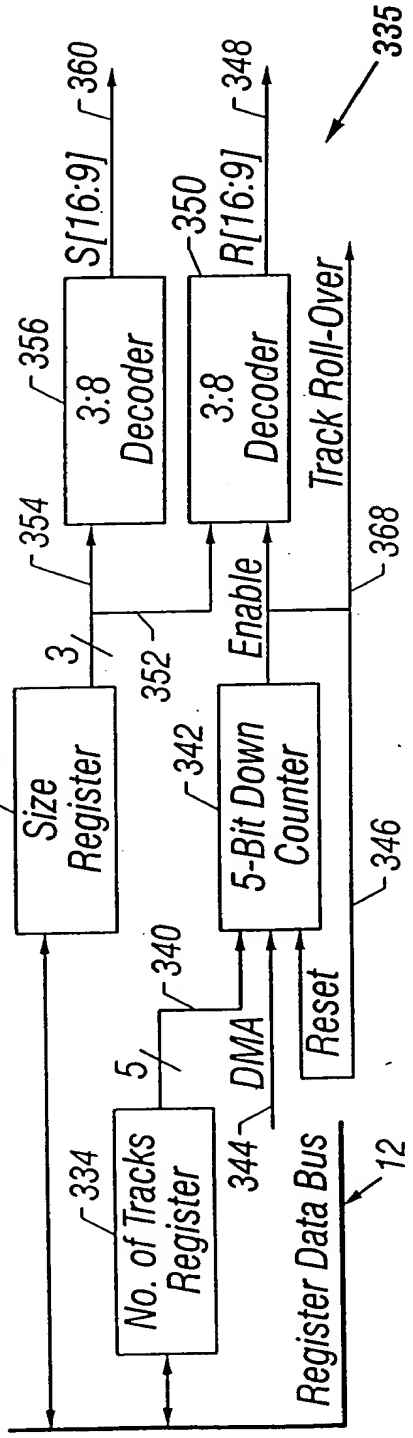
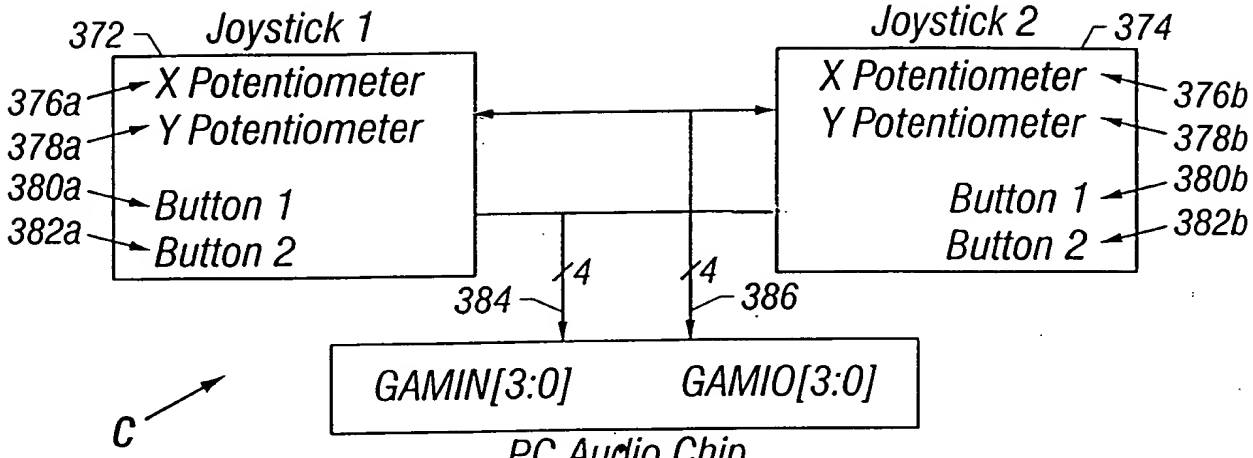

335
360
S[16:9]
348
R[16:9]
350
356
3:8 Decoder
3:8 Decoder
Track Roll-Over
354
368
3
352
Enable
336
Size Register
342
5-Bit Down Counter
346
340
5
DMA
Reset
334
No. of Tracks Register
344
12
Register Data Bus

FIG. 39B



System Configuration

FIG. 40

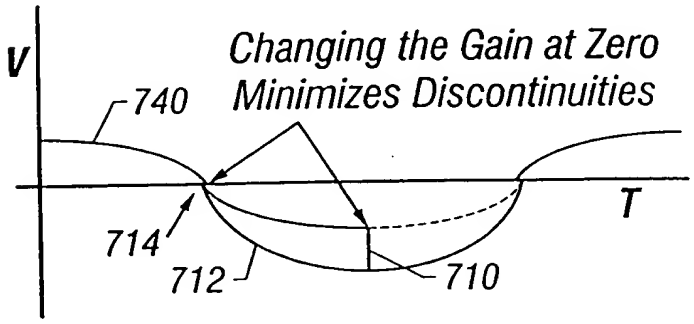


FIG. 46

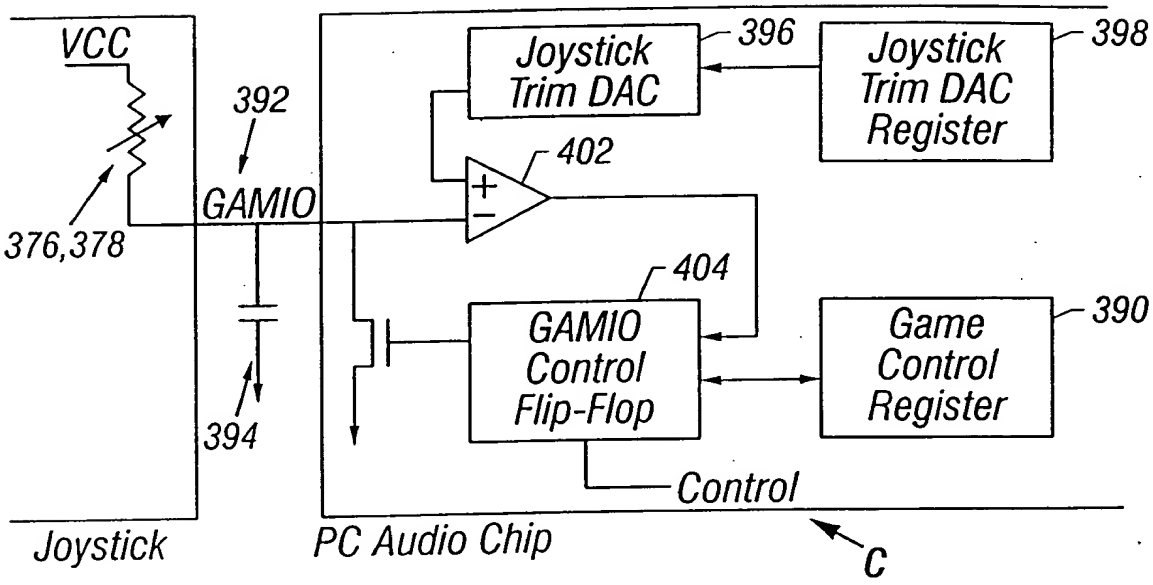


FIG. 41A

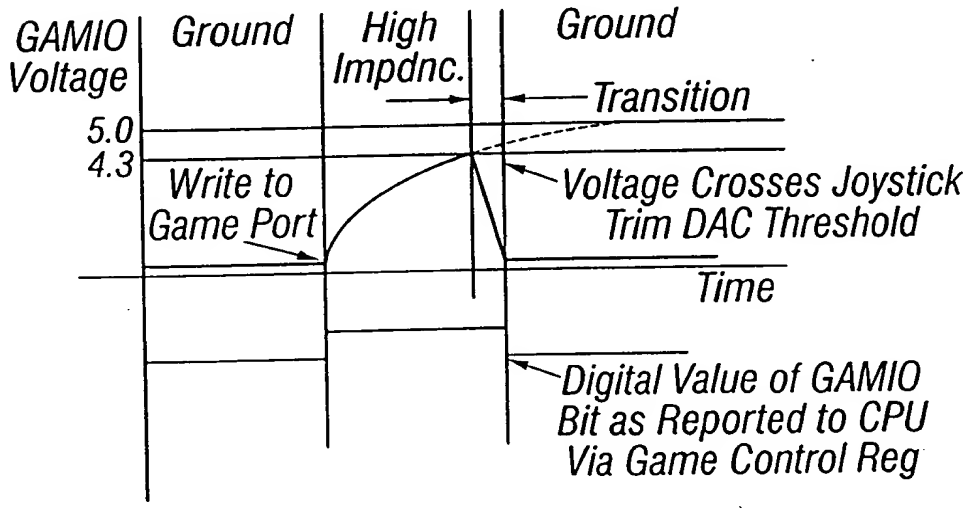


FIG. 41B

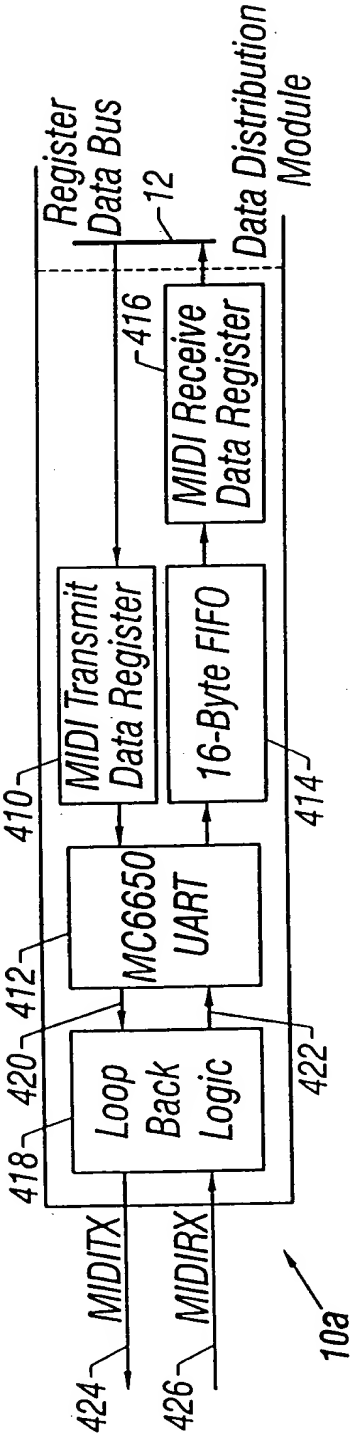

Register Data Bus
12
Data Distribution Module
MIDI Receive Data Register
416
MIDI Transmit Data Register
16-Byte FIFO
410
414
MC6650 UART
412
420
Loop Back Logic
422
418
MIDITX
MIDIRX
424
426
10a

FIG. 42

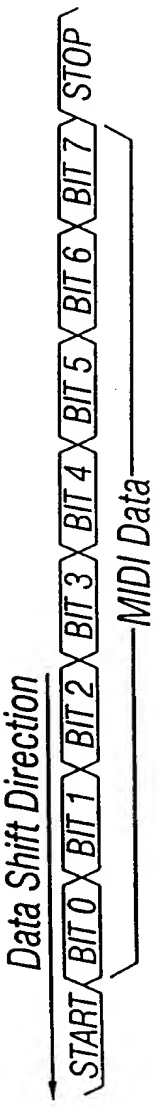

Data Shift Direction
START
BIT 0
BIT 1
BIT 2
BIT 3
BIT 4
BIT 5
BIT 6
BIT 7
STOP
MIDI Data

FIG. 43

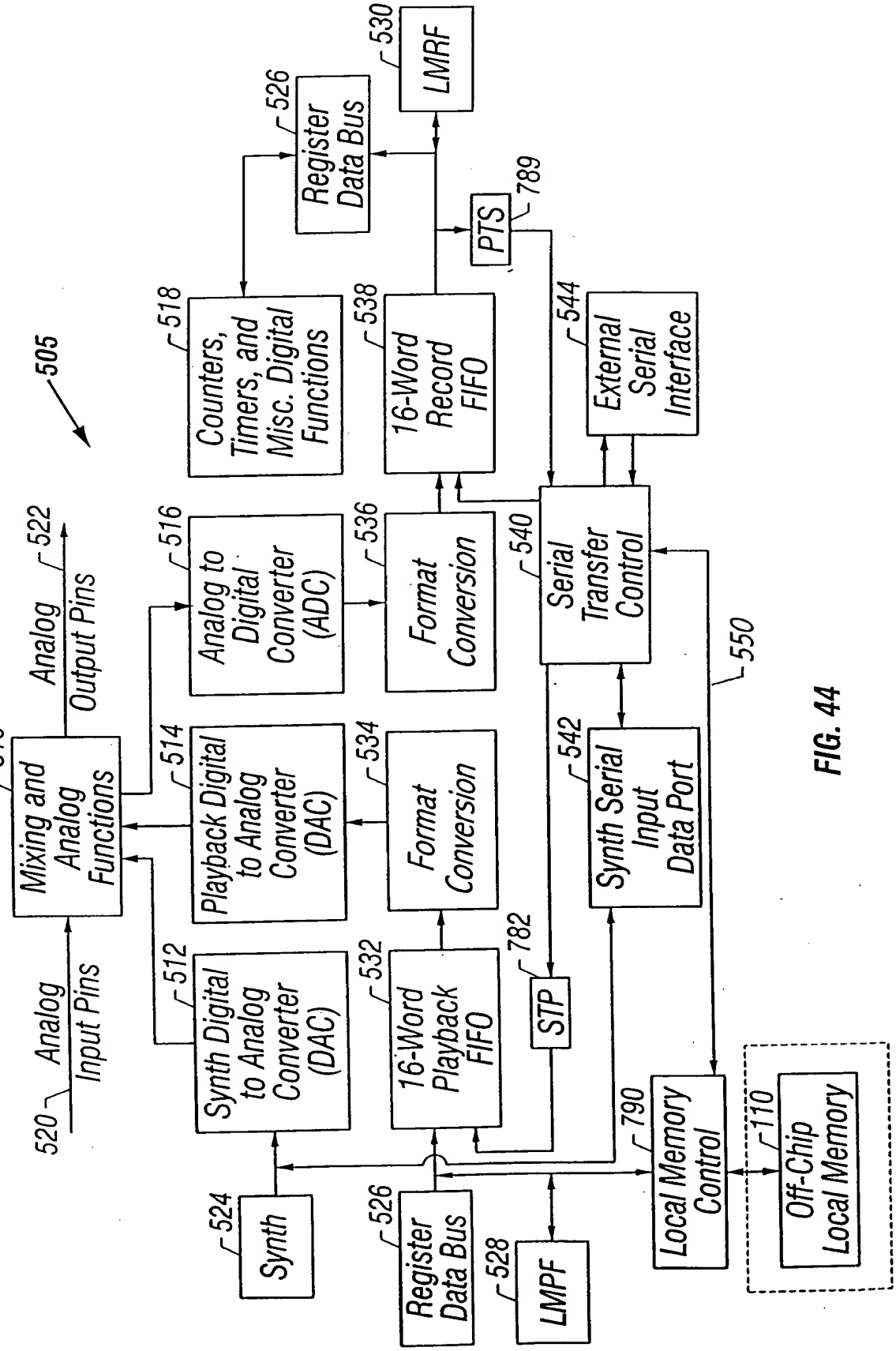

505
Mixing and Analog Functions
510
Analog Input Pins
520
Analog Output Pins
522
Synth Digital to Analog Converter (DAC)
512
Playback Digital to Analog Converter (DAC)
514
Analog to Digital Converter (ADC)
516
Synth
524
Register Data Bus
526
LMPF
528
Register Data Bus
526
LMRF
530
16-Word Playback FIFO
532
Format Conversion
534
Format Conversion
536
16-Word Record FIFO
538
STP
782
PTS
789
Counters, Timers, and Misc. Digital Functions
518
Serial Transfer Control
540
Synth Serial Input Data Port
542
External Serial Interface
544
550
Local Memory Control
790
Off-Chip Local Memory
110

FIG. 44

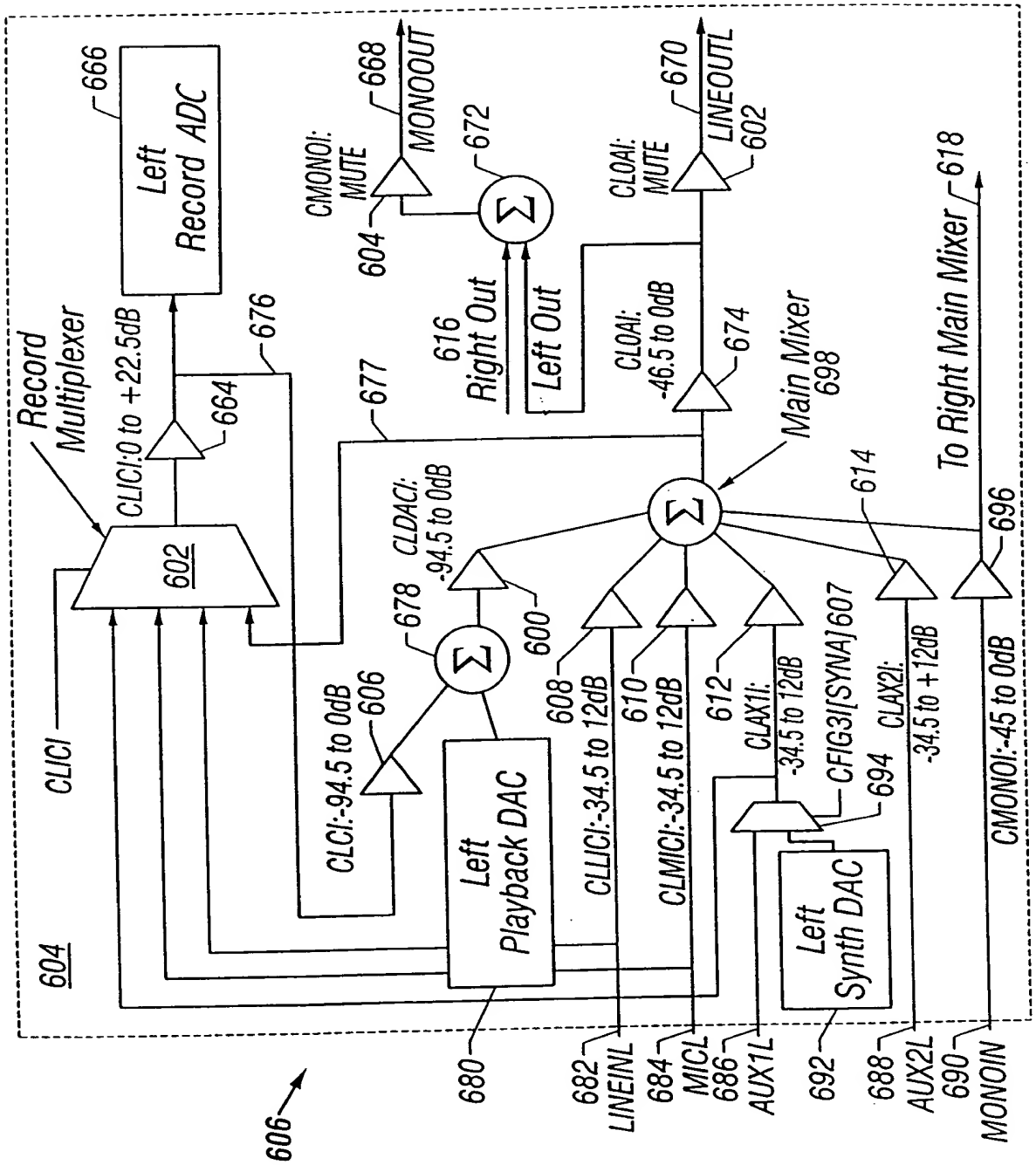

604
Record Multiplexer
602
CLICI
CLICI:0 to +22.5dB
664
666
Left Record ADC
676
677
CLCI:-94.5 to 0dB
606
678
CLDACI: -94.5 to 0dB
600
Left Playback DAC
680
CLLICI:-34.5 to 12dB
682
LINEINL
CLMICI:-34.5 to 12dB
684
MICL
CLAX1I: -34.5 to 12dB
686
AUX1L
CFIG3/SYNA 607
694
Left Synth DAC
692
CLAX2I: -34.5 to +12dB
688
AUX2L
CMONOI:-45 to 0dB
690
MONOIN
608
610
612
614
Main Mixer 698
674
CLOAI: -46.5 to 0dB
CLOAI: MUTE
670
LINEOUTL
602
672
616 Right Out
Left Out
CMONOI: MUTE
668
MONOOUT
604
To Right Main Mixer
618
696
606

FIG. 45A

0 to +22.5dB (4-bit) gain table							
Value	dB	Value	dB	Value	dB	Value	dB
00h	00.0	04h	+06.0	08h	+12.0	0Ch	+18.0
01h	+01.5	05h	+07.5	09h	+13.5	0Dh	+19.5
02h	+03.0	06h	+09.0	0Ah	+15.0	0Eh	+21.0
03h	+04.5	07h	+10.5	0Bh	+16.5	0Fh	+22.5

0 to -45.0dB (4-bit) attenuation table							
Value	dB	Value	dB	Value	dB	Value	dB
00h	00.0	04h	-12.0	08h	-24.0	0Ch	-36.0
01h	-03.0	05h	-15.0	09h	-27.0	0Dh	-39.0
02h	-06.0	06h	-18.0	0Ah	-30.0	0Eh	-42.0
03h	-09.0	07h	-21.0	0Bh	-33.0	0Fh	-45.0

12 to -34.5dB (5-bit) gain attenuation table							
Value	dB	Value	dB	Value	dB	Value	dB
00h	+12.0	08h	00.0	10h	-12.0	18h	-24.0
01h	+10.5	09h	-01.5	11h	-13.5	19h	-25.5
02h	+09.0	0Ah	-03.0	12h	-15.0	1Ah	-27.0
03h	+07.5	0Bh	-04.5	13h	-16.5	1Bh	-28.5
04h	+06.0	0Ch	-06.0	14h	-18.0	1Ch	-30.0
05h	+04.5	0Dh	-07.5	15h	-19.5	1Dh	-31.5
06h	+03.0	0Eh	-09.0	16h	-21.0	1Eh	-33.0
07h	+01.5	0Fh	-10.5	17h	-22.5	1Fh	-34.5

FIG. 45B-1

REPLACEMENT SHEET

0 to -46.5dB (5-bit) attenuation table for CLOAI and CROAI							
Value	dB	Value	dB	Value	dB	Value	dB
00h	00.0	08h	-12.0	10h	-24.0	18h	-36.0
01h	-01.5	09h	-13.5	11h	-25.5	19h	-37.5
02h	-03.0	0Ah	-15.0	12h	-27.0	1Ah	-39.0
03h	-04.5	0Bh	-16.5	13h	-28.5	1Bh	-40.5
04h	-06.0	0Ch	-18.0	14h	-30.0	1Ch	-42.0
05h	-07.5	0Dh	-19.5	15h	-31.5	1Dh	-43.5
06h	-09.0	0Eh	-21.0	16h	-33.0	1Eh	-45.0
07h	-10.5	0Fh	-22.5	17h	-34.5	1Fh	-46.5

0 to -94.5dB (6-bit) attenuation table							
Value	dB	Value	dB	Value	dB	Value	dB
00h	00.0	10h	-24.0	20h	-48.0	30h	-72.0
01h	-01.5	11h	-25.5	21h	-49.5	31h	-73.5
02h	-03.0	12h	-27.0	22h	-51.0	32h	-75.0
03h	-04.5	13h	-28.5	23h	-52.5	33h	-76.5
04h	-06.0	14h	-30.0	24h	-54.0	34h	-78.0
05h	-07.5	15h	-31.5	25h	-55.5	35h	-79.5
06h	-09.0	16h	-33.0	26h	-57.0	36h	-81.0
07h	-10.5	17h	-34.5	27h	-58.5	37h	-82.5
08h	-12.0	18h	-36.0	28h	-60.0	38h	-84.0
09h	-13.5	19h	-37.5	29h	-61.5	39h	-85.5
0Ah	-15.0	1Ah	-39.0	2Ah	-63.0	3Ah	-87.0
0Bh	-16.5	1Bh	-40.5	2Bh	-64.5	3Bh	-88.5
0Ch	-18.0	1Ch	-42.0	2Ch	-66.0	3Ch	-90.0
0Dh	-19.5	1Dh	-43.5	2Dh	-67.5	3Dh	-91.5
0Eh	-21.0	1Eh	-45.0	2Eh	-69.0	3Eh	-93.0
0Fh	-22.5	1Fh	-46.5	2Fh	-70.5	3Fh	-94.5

FIG. 45B-2

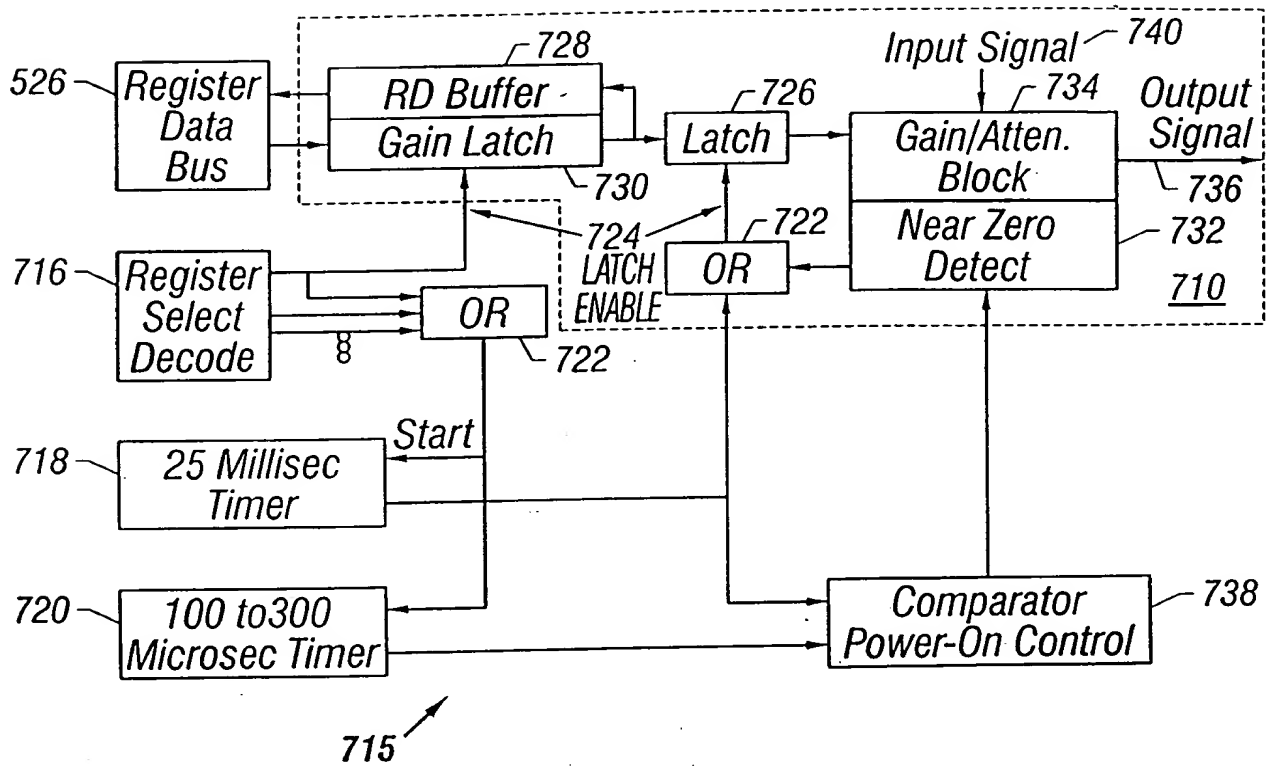

526
Register Data Bus
728
RD Buffer
Gain Latch
730
726
Latch
Input Signal
740
734
Gain/Atten. Block
Output Signal
736
Near Zero Detect
732
710
724
LATCH ENABLE
722
OR
716
Register Select Decode
OR
722
Start
718
25 Millisec Timer
720
100 to300 Microsec Timer
Comparator Power-On Control
738
715

FIG. 47

REPLACEMENT SHEET

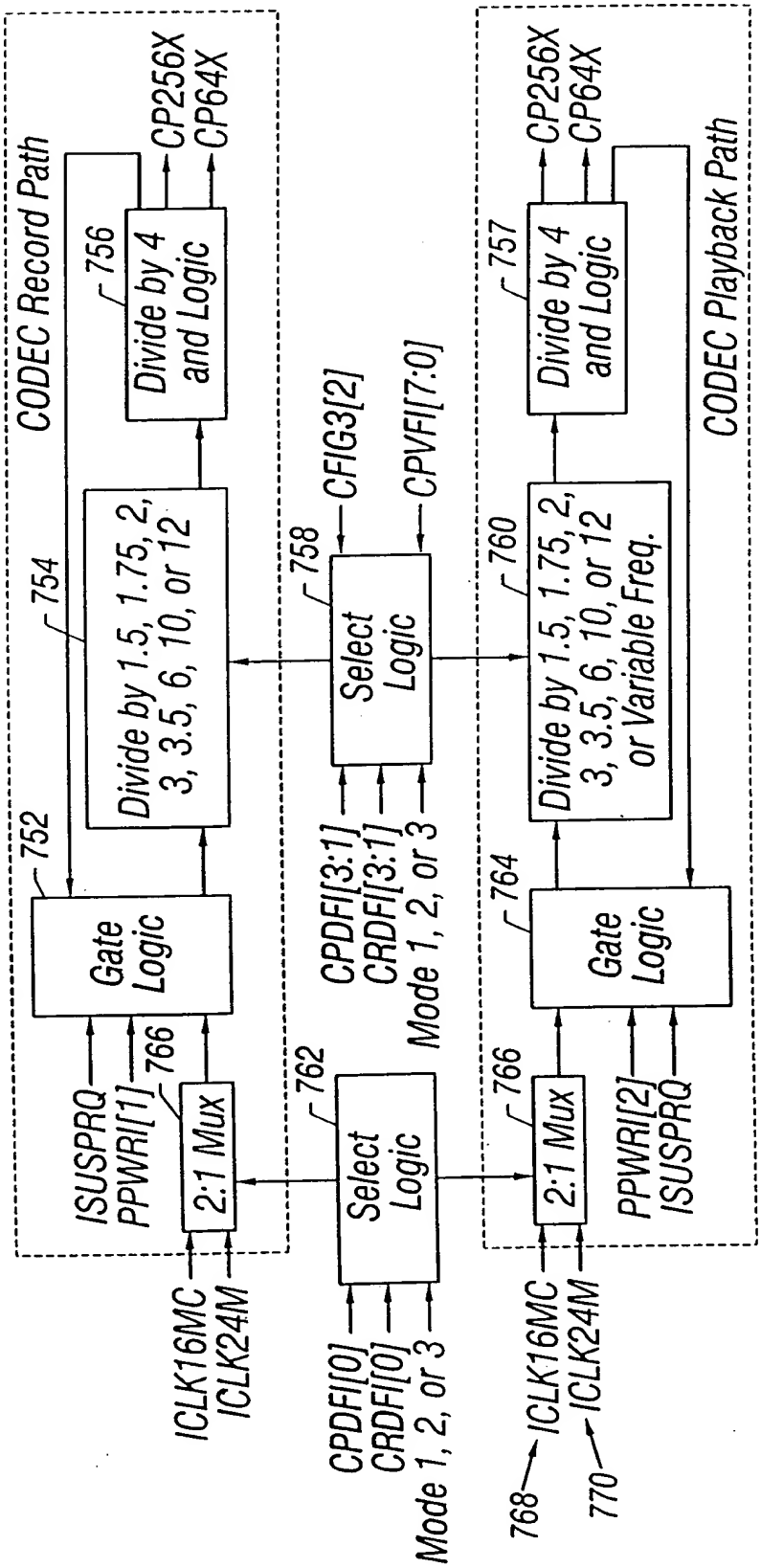


FIG. 48

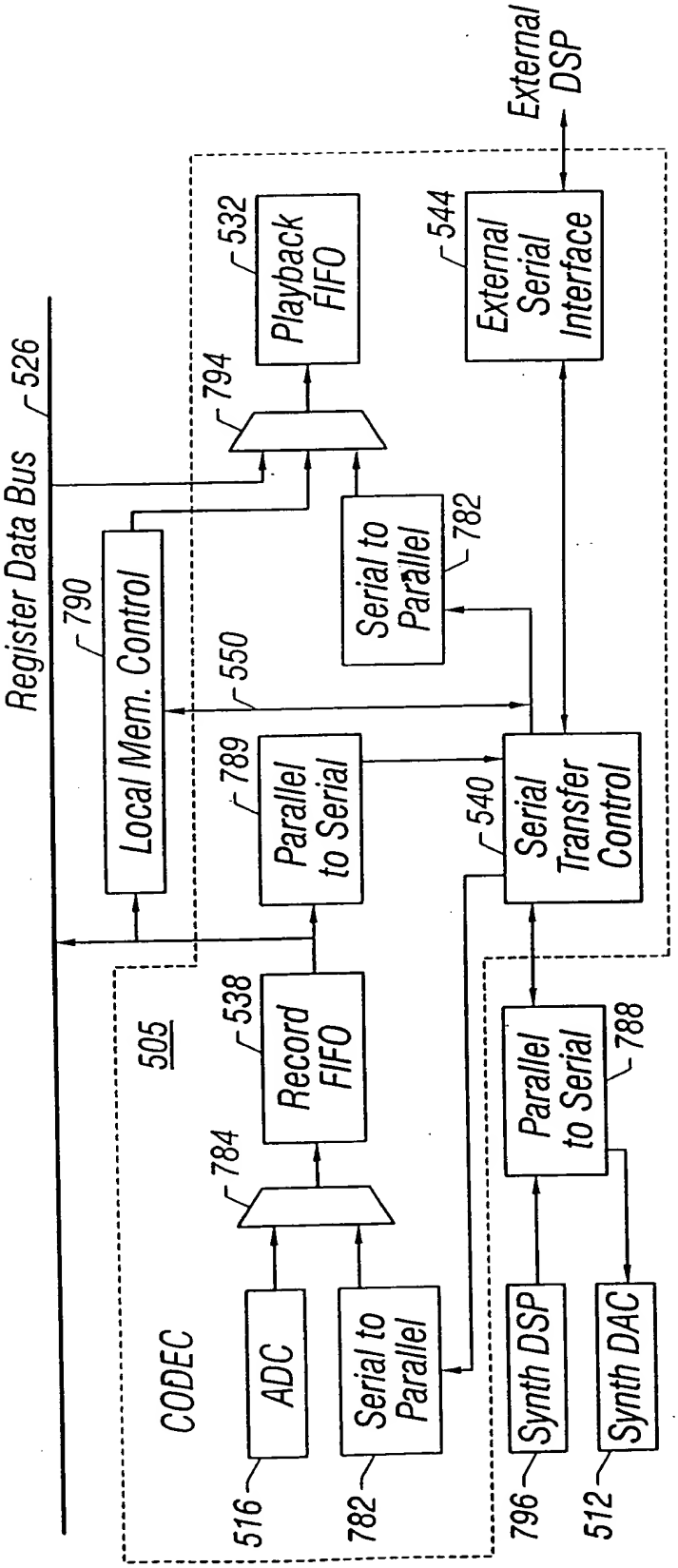

External DSP
532
Playback FIFO
544
External Serial Interface
794
526
Register Data Bus
790
Local Mem. Control
782
Serial to Parallel
550
789
Parallel to Serial
540
Serial Transfer Control
505
538
Record FIFO
788
Parallel to Serial
784
CODEC
ADC
Serial to Parallel
Synth DSP
Synth DAC
516
782
796
512

FIG. 49A

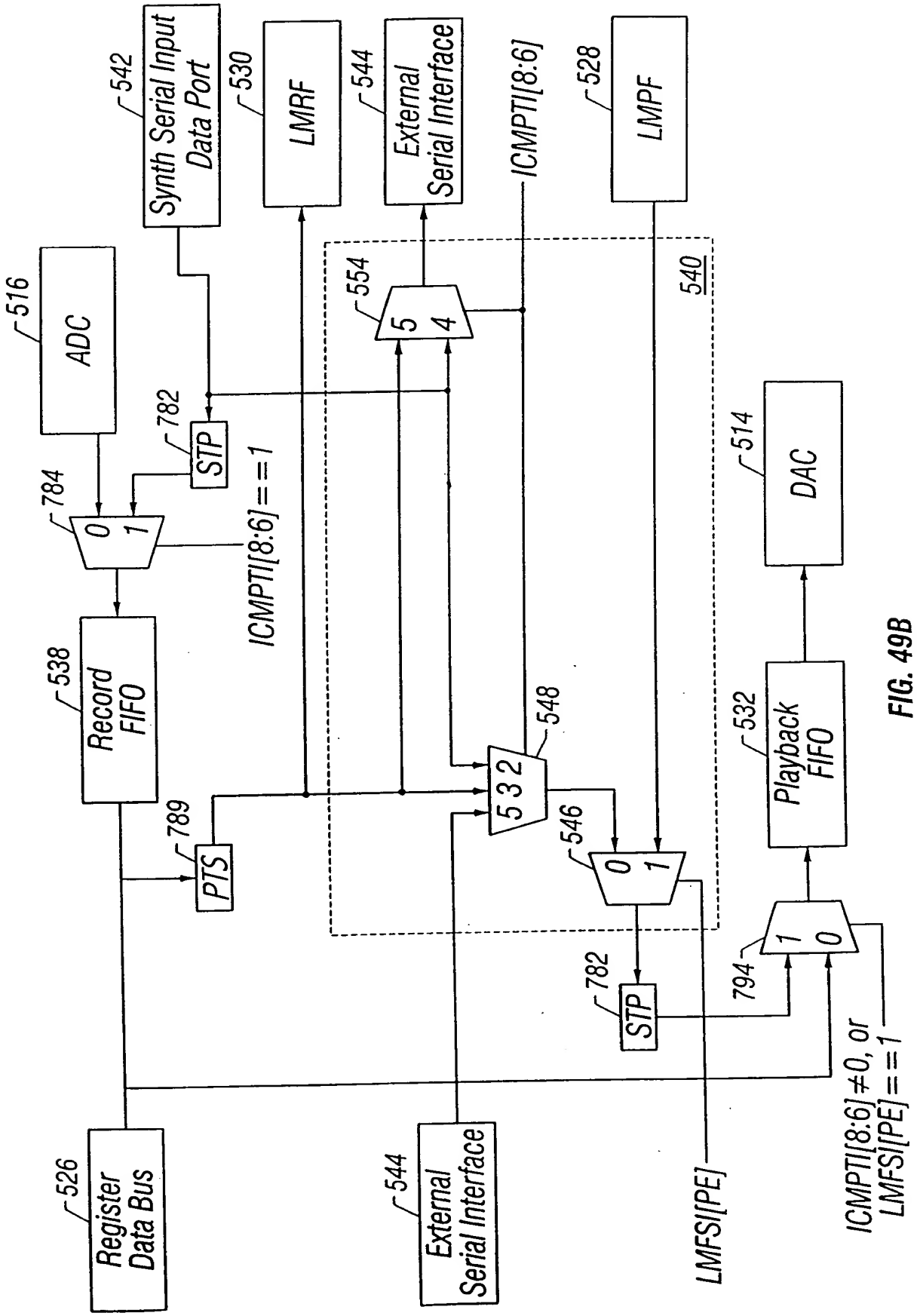

542
Synth Serial Input Data Port
530
LMRF
544
External Serial Interface
ICMPTI[8:6]
528
LMPF
516
ADC
554
5 4
540
782
STP
784
0 1
ICMPTI[8:6] == 1
514
DAC
538
Record FIFO
548
5 3 2
532
Playback FIFO
789
PTS
546
0 1
782
STP
794
1 0
526
Register Data Bus
544
External Serial Interface
LMFSI[PE]
ICMPTI[8:6] ≠ 0, or
LMFSI[PE] == 1

FIG. 49B

REPLACEMENT SHEET

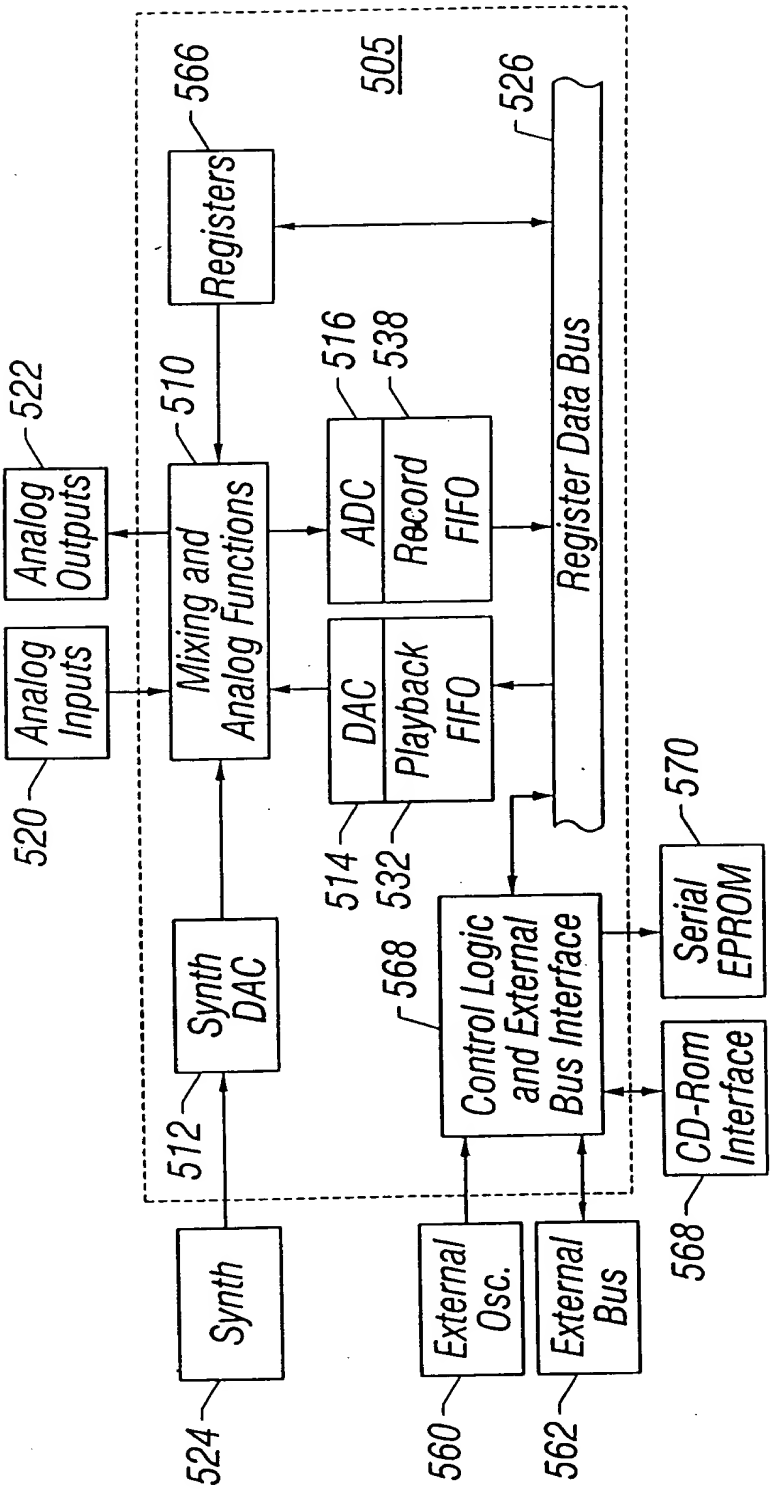


FIG. 50

REPLACEMENT SHEET

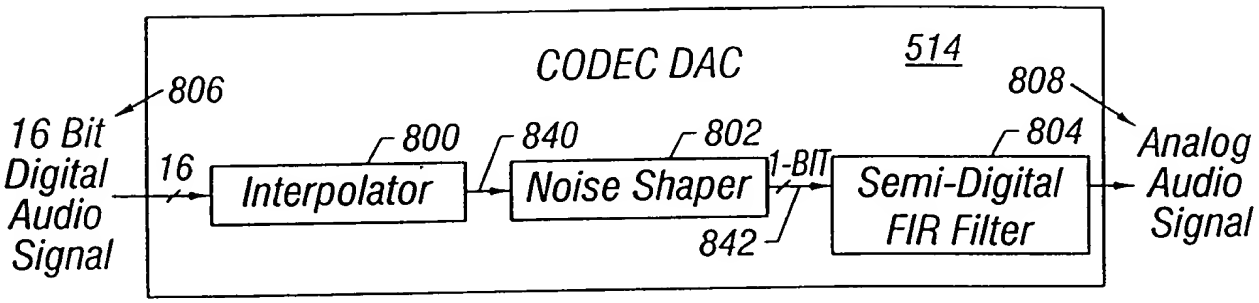


FIG. 51

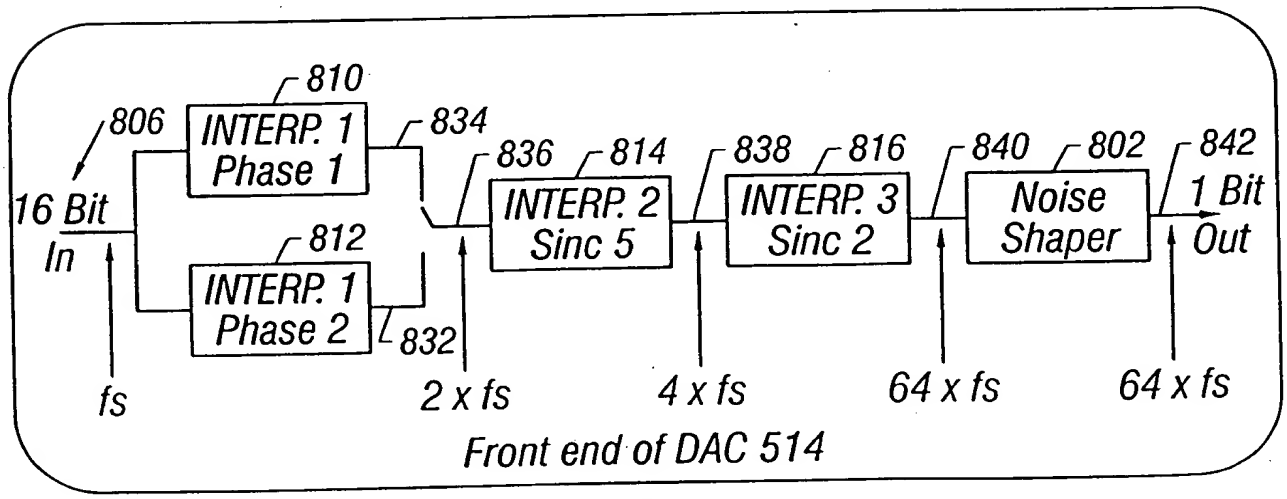


FIG. 52

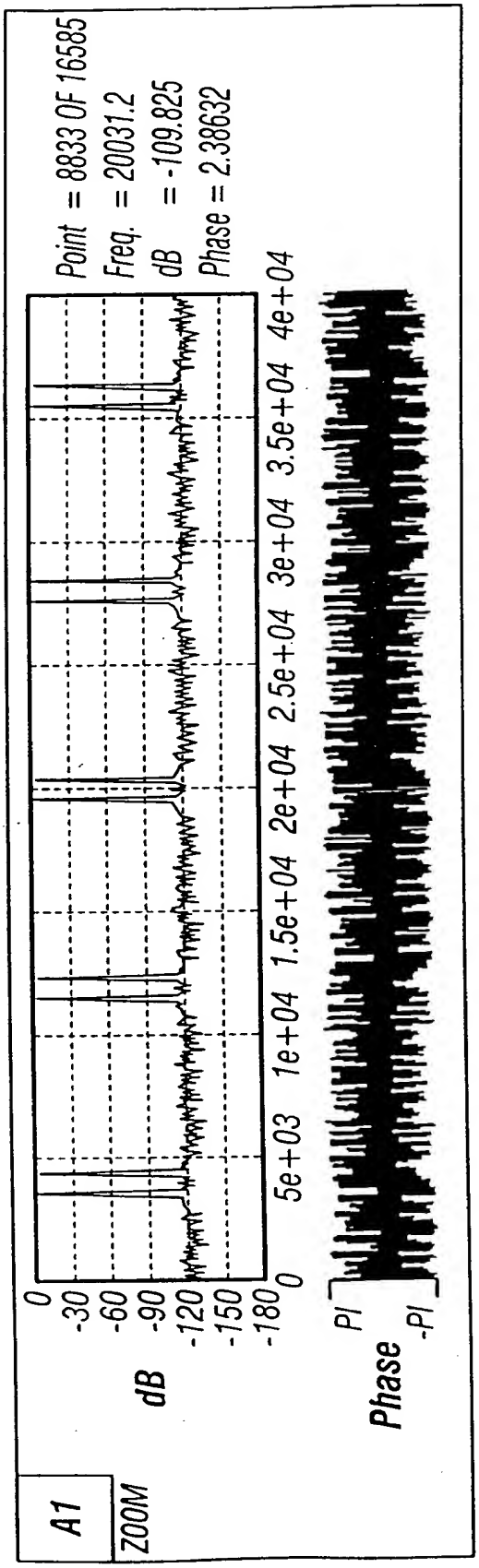


FIG. 53A

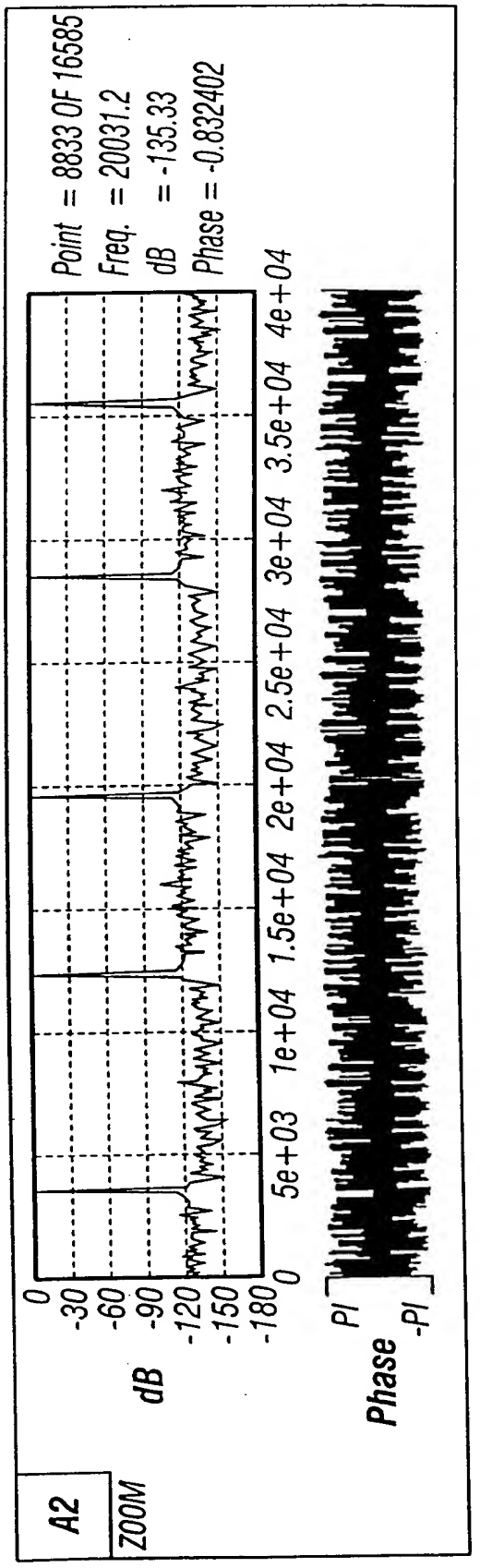


FIG. 53B

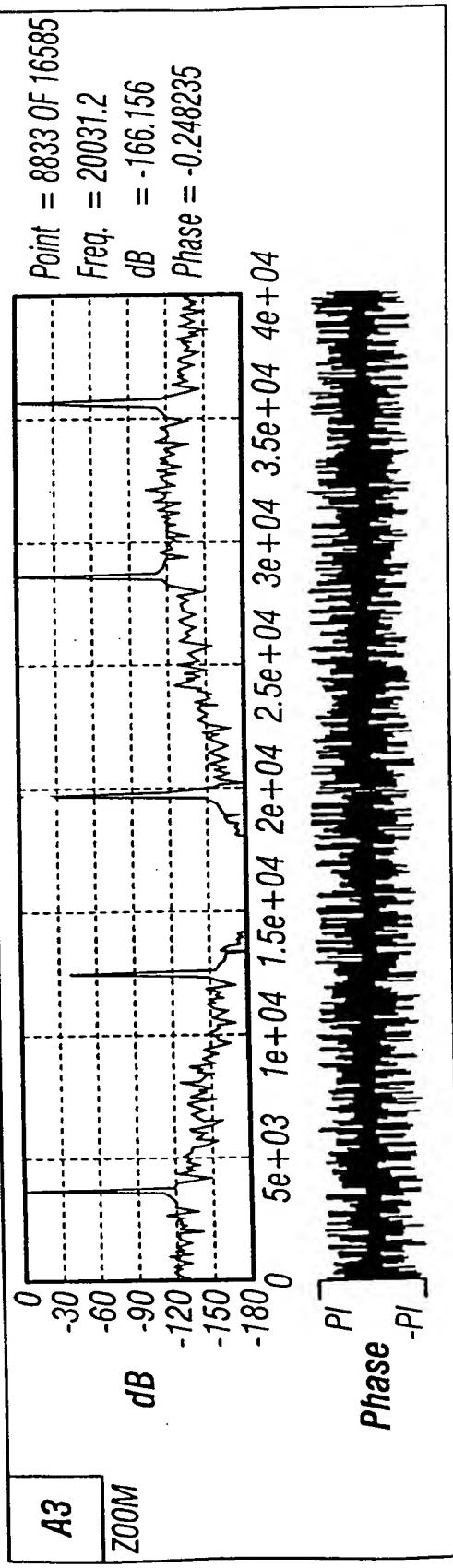


FIG. 53C

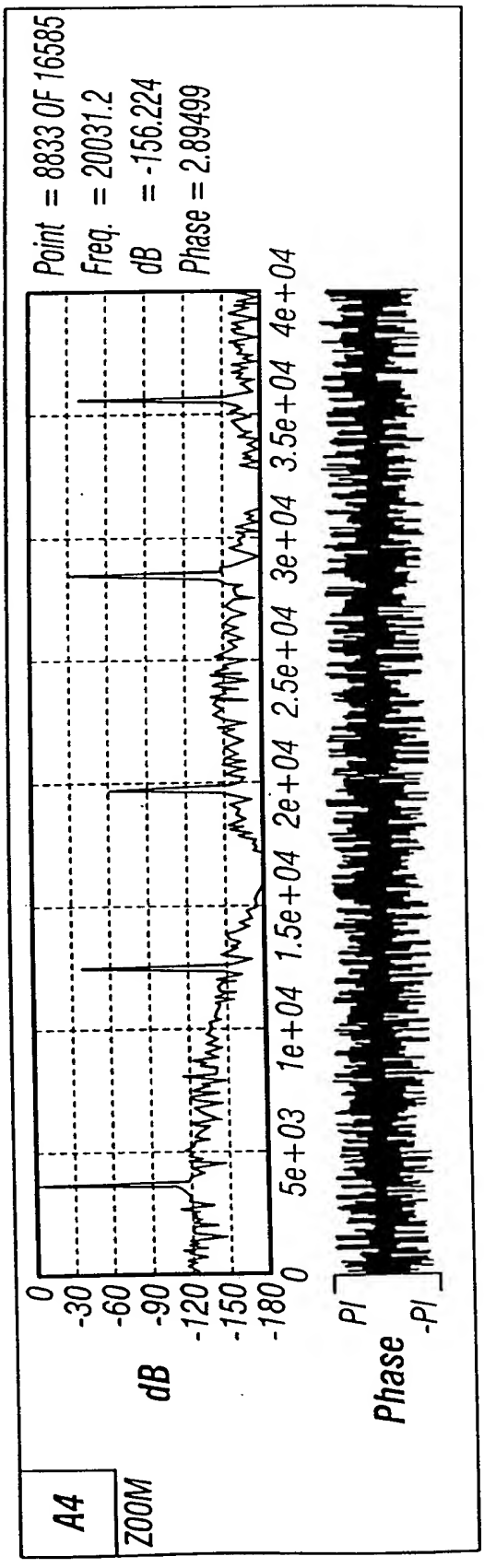


FIG. 53D

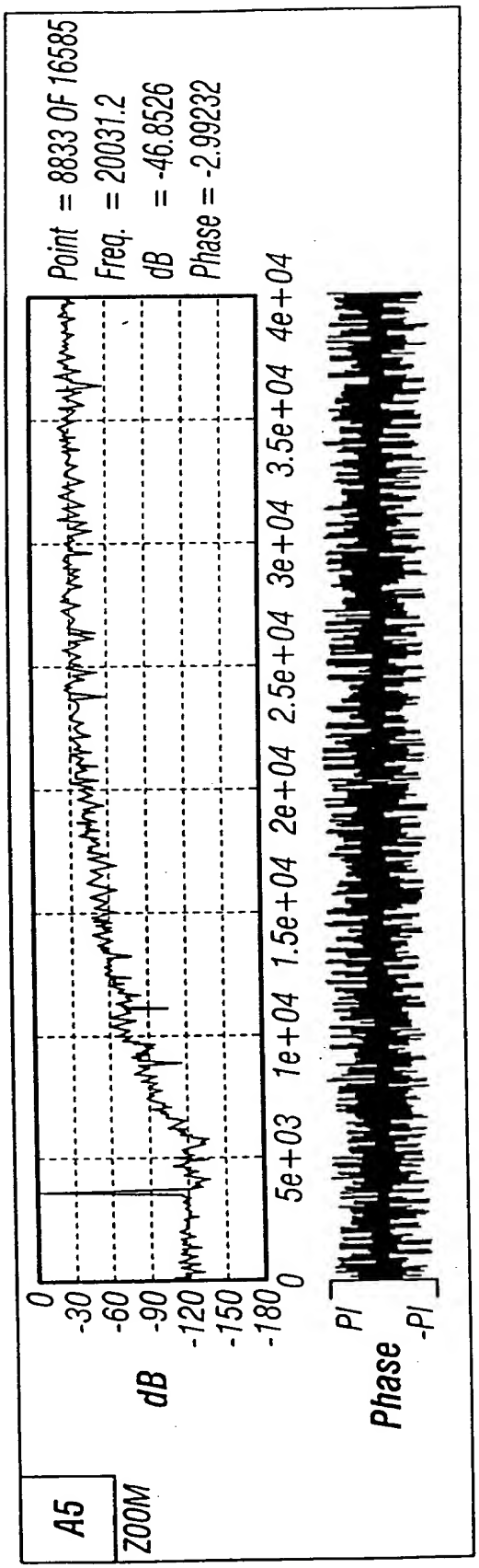


FIG. 53E

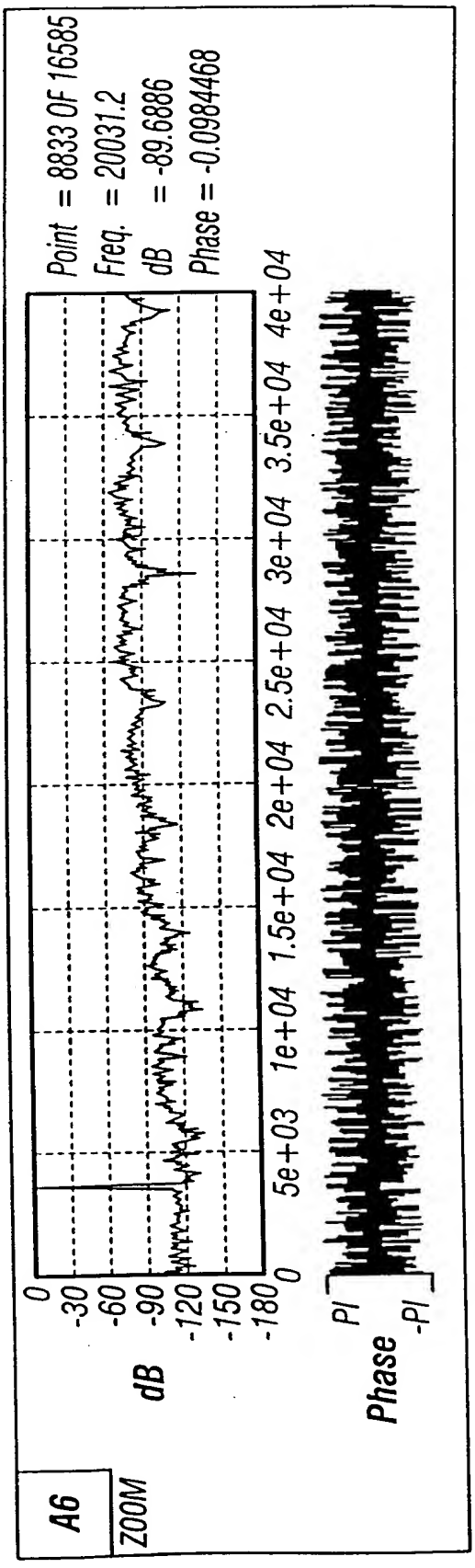


FIG. 53F

REPLACEMENT SHEET

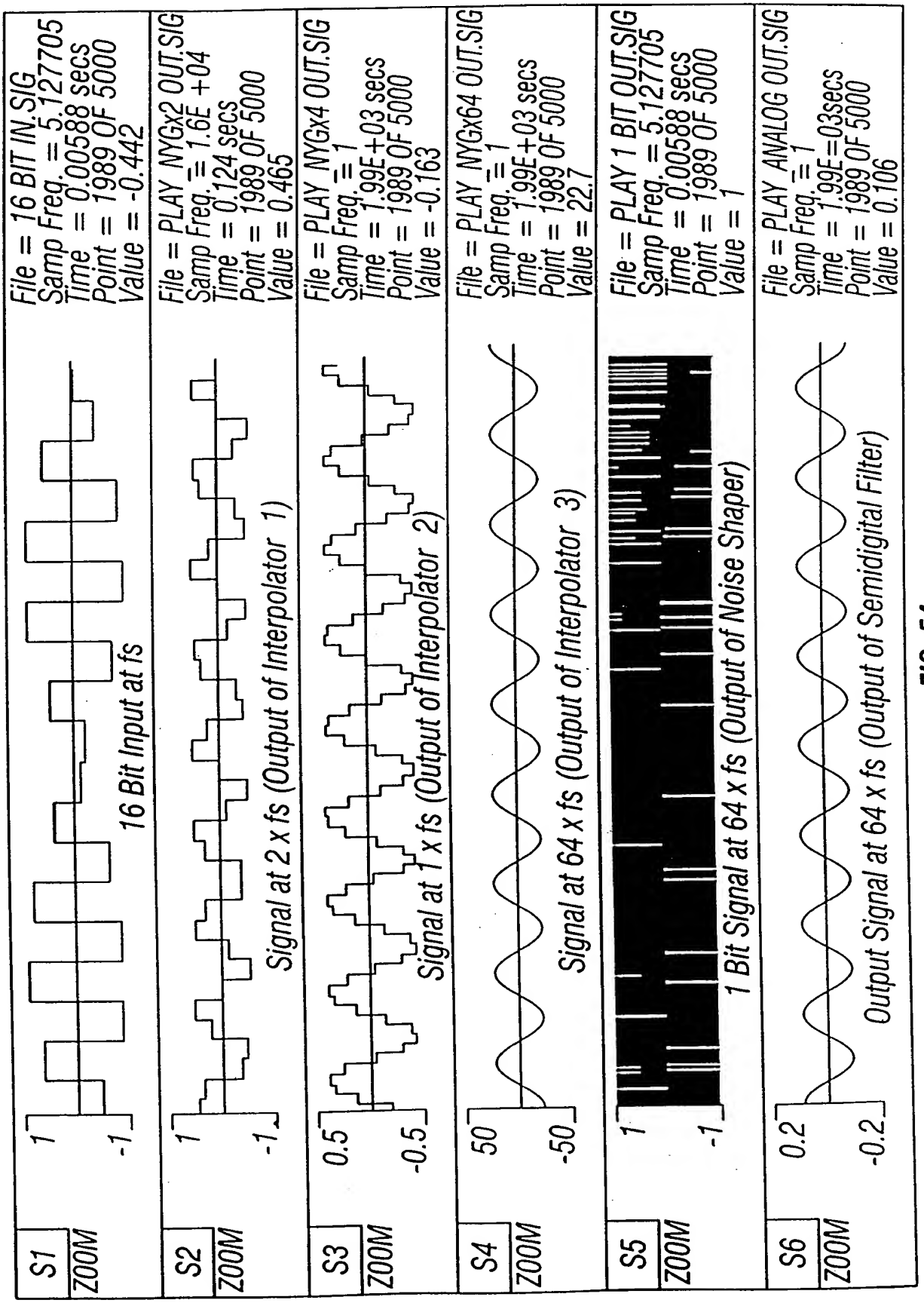


FIG. 54

REPLACEMENT SHEET

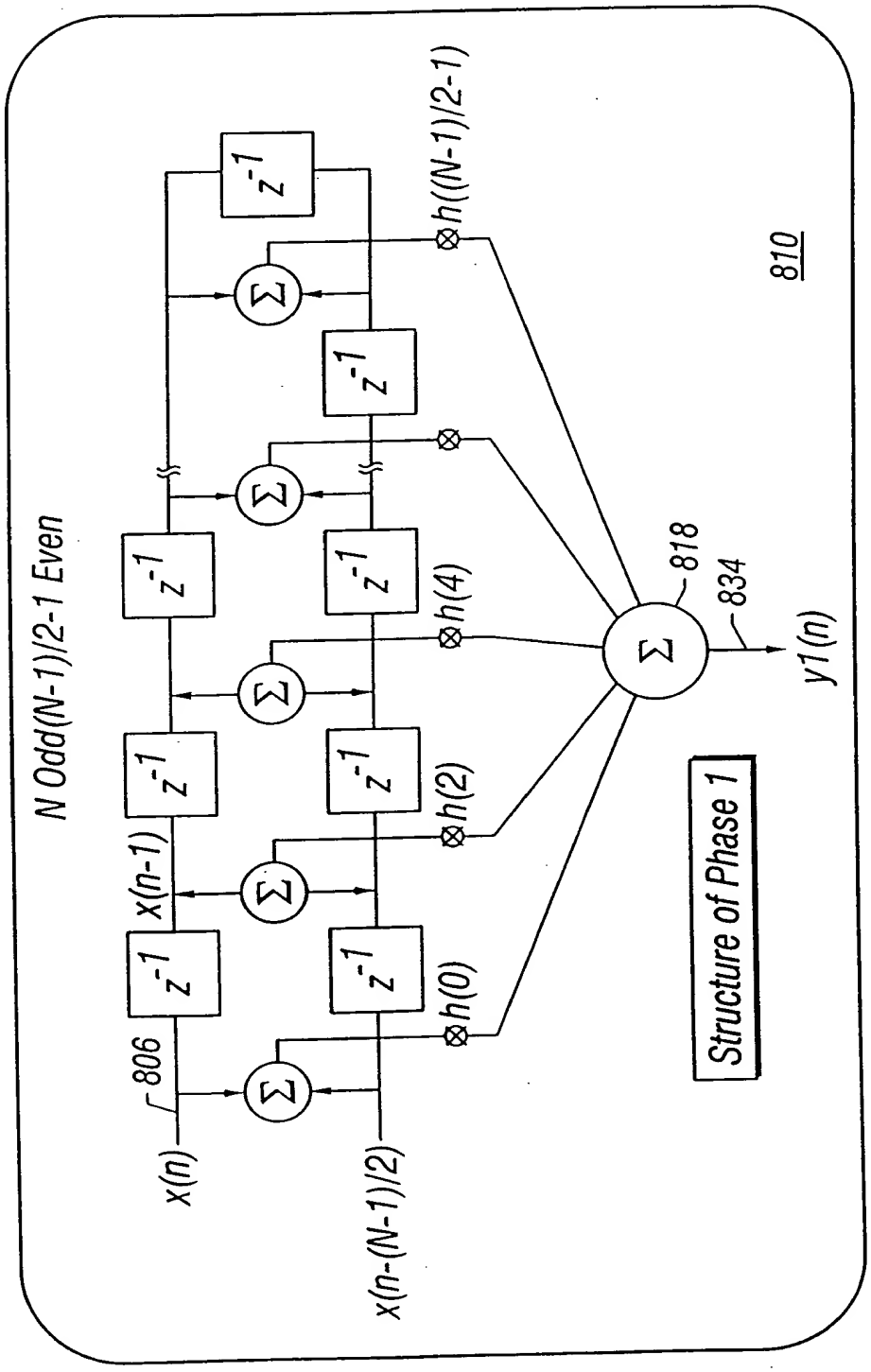


FIG. 55

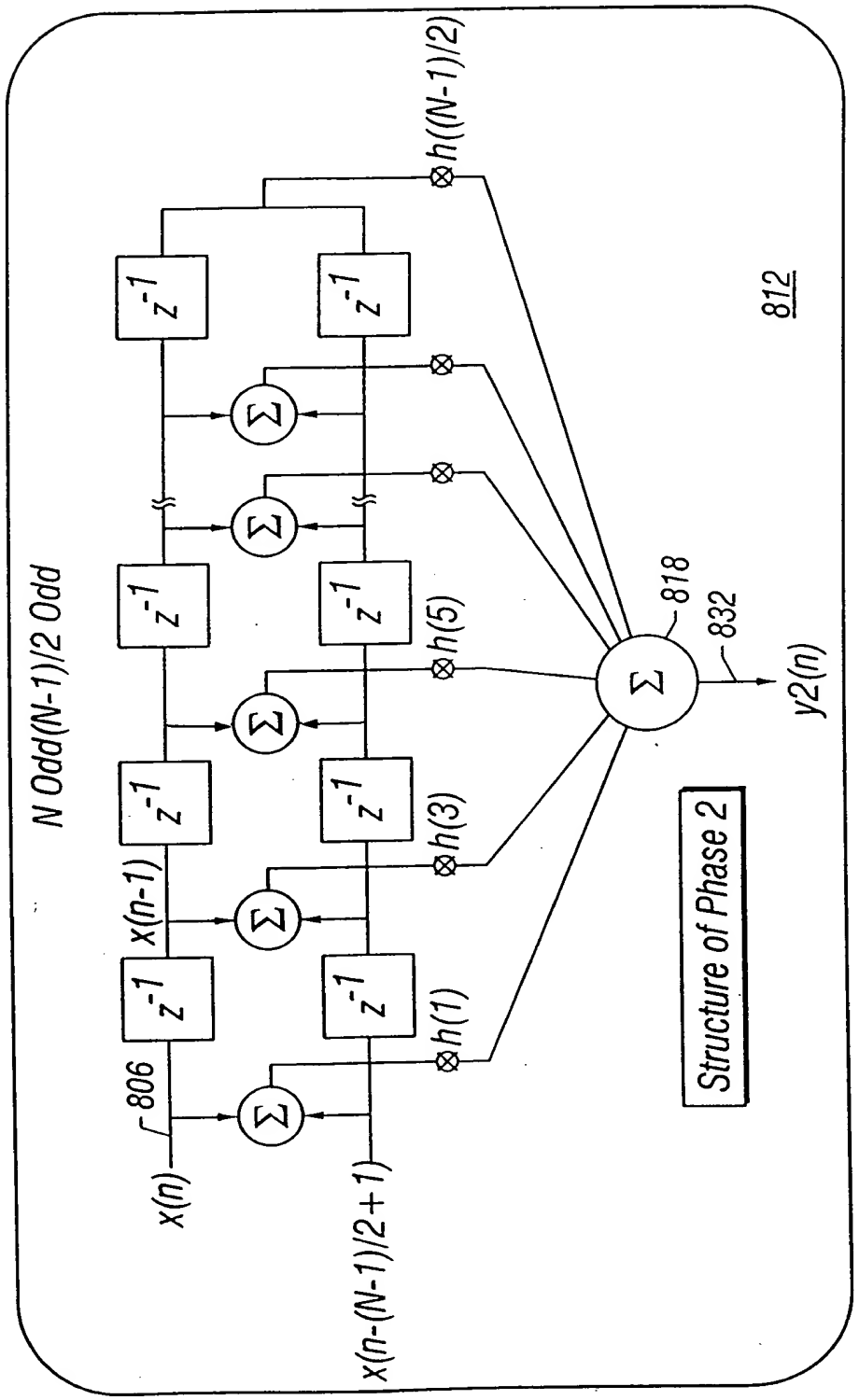

N Odd(N-1)/2 Odd
h((N-1)/2)
812
818
832
y2(n)
h(5)
h(3)
h(1)
x(n-1)
806
x(n)
x(n-(N-1)/2+1)
Structure of Phase 2

FIG. 56

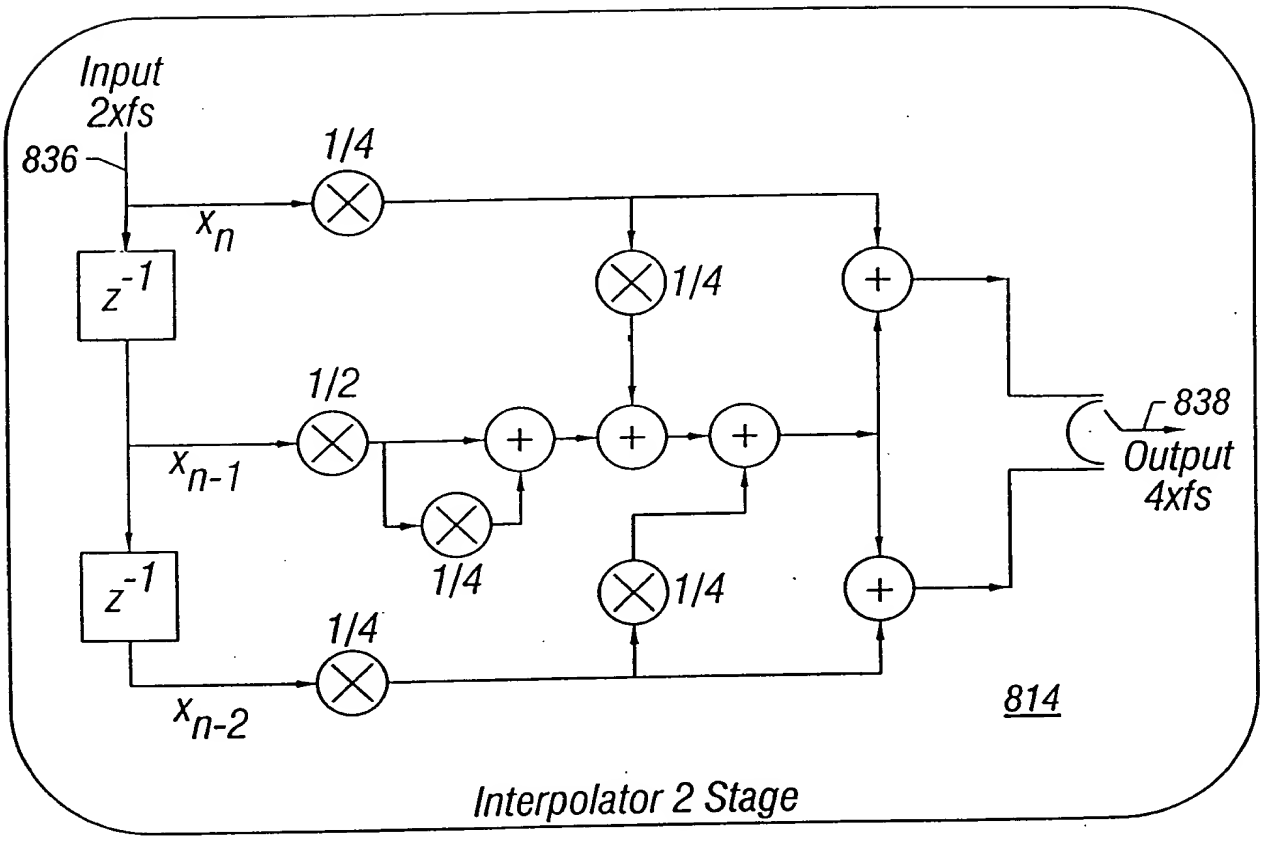

Input
2xfs
836
1/4
x_n
z^{-1}
1/4
1/2
x_{n-1}
838
Output
4xfs
1/4
z^{-1}
1/4
1/4
x_{n-2}
814
Interpolator 2 Stage

FIG. 57

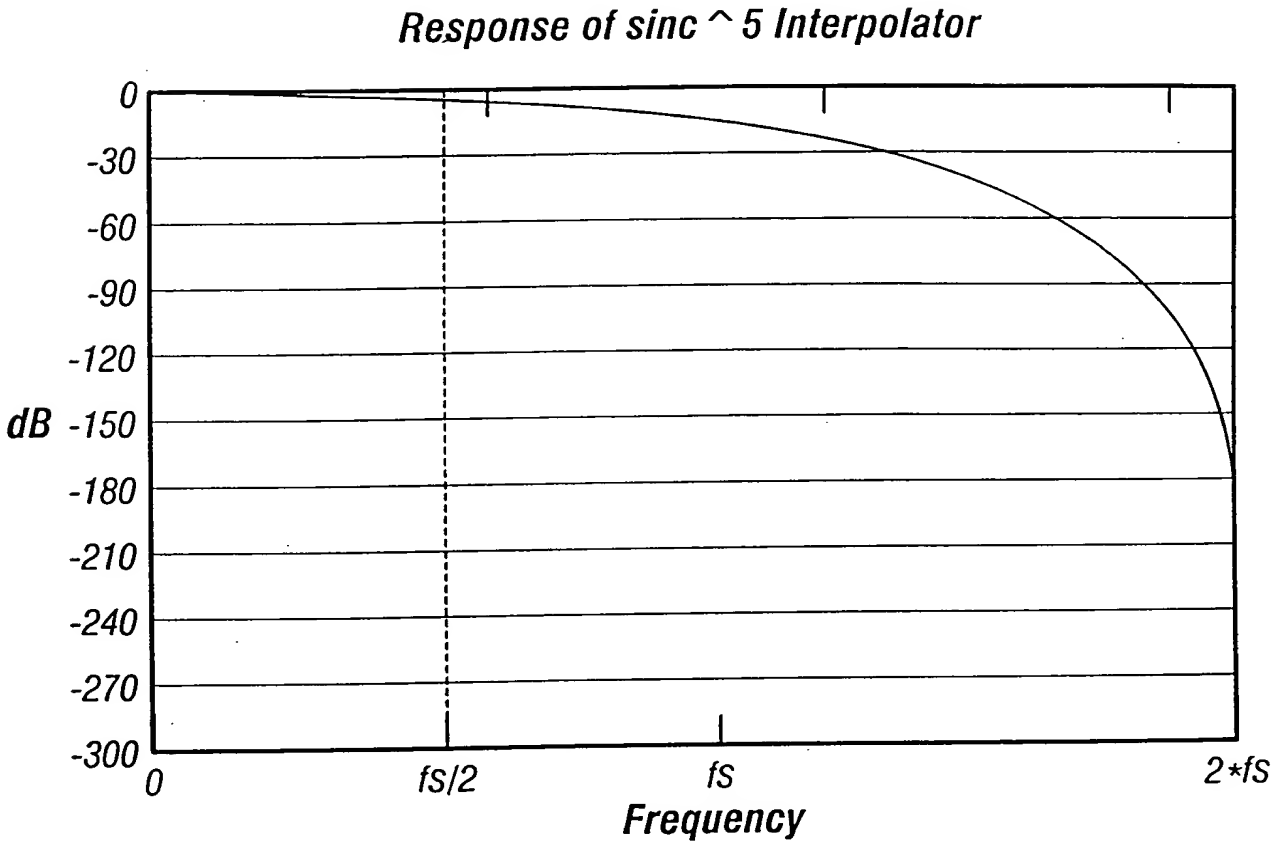

Response of sinc ^ 5 Interpolator
0
-30
-60
-90
-120
dB -150
-180
-210
-240
-270
-300
0
fs/2
fs
2*fs
Frequency

FIG. 58

REPLACEMENT SHEET

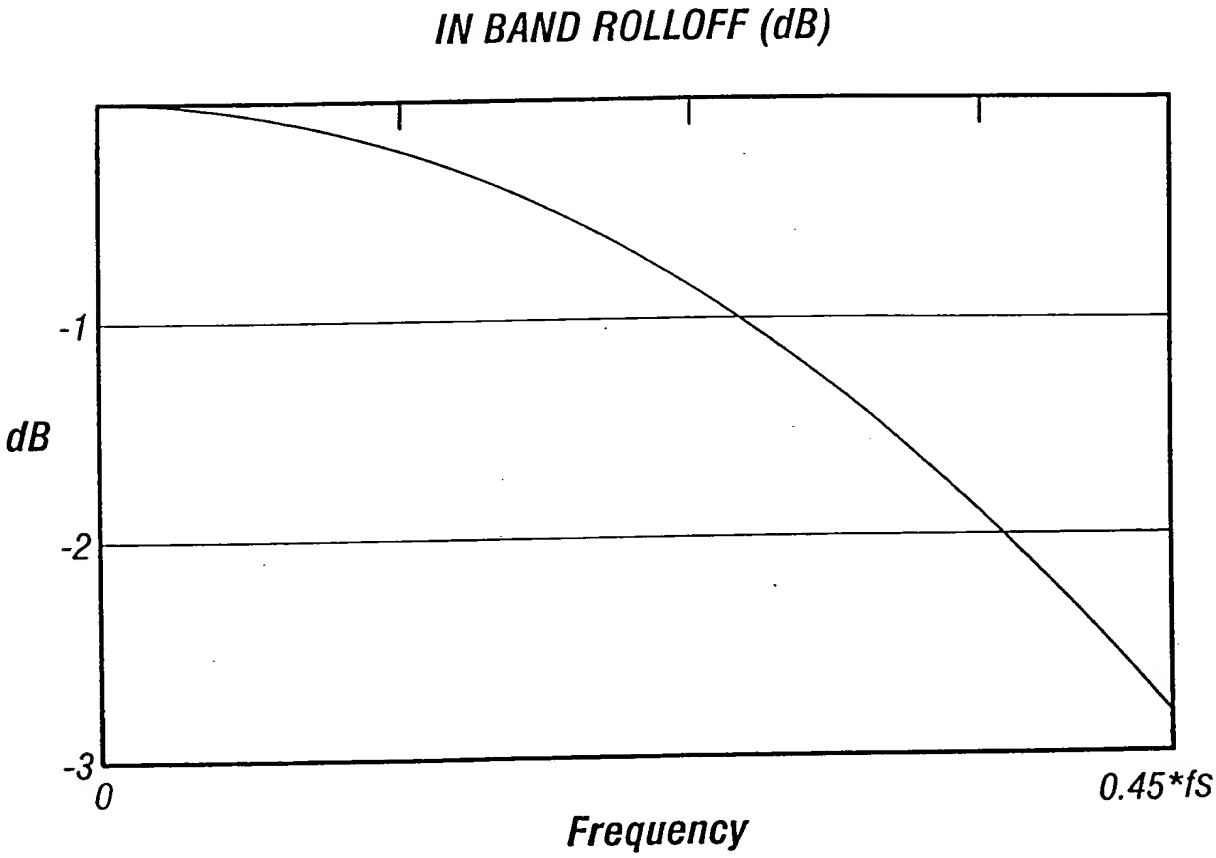


FIG. 59

REPLACEMENT SHEET

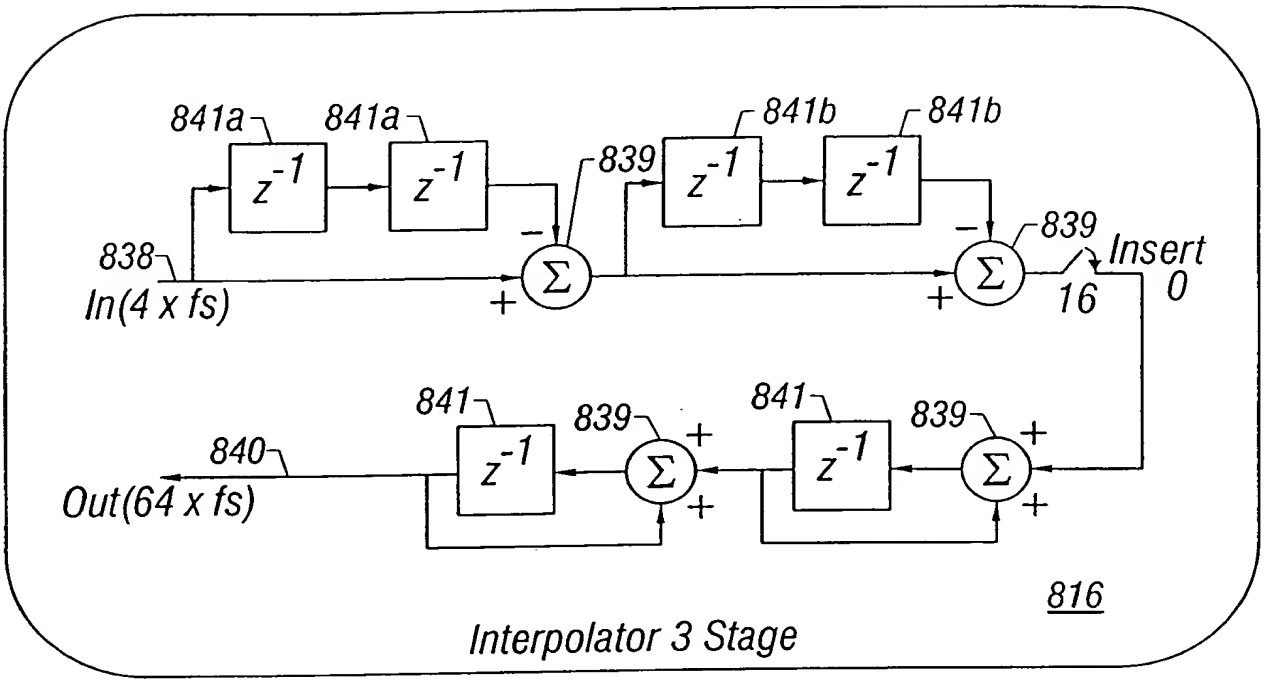


FIG. 60

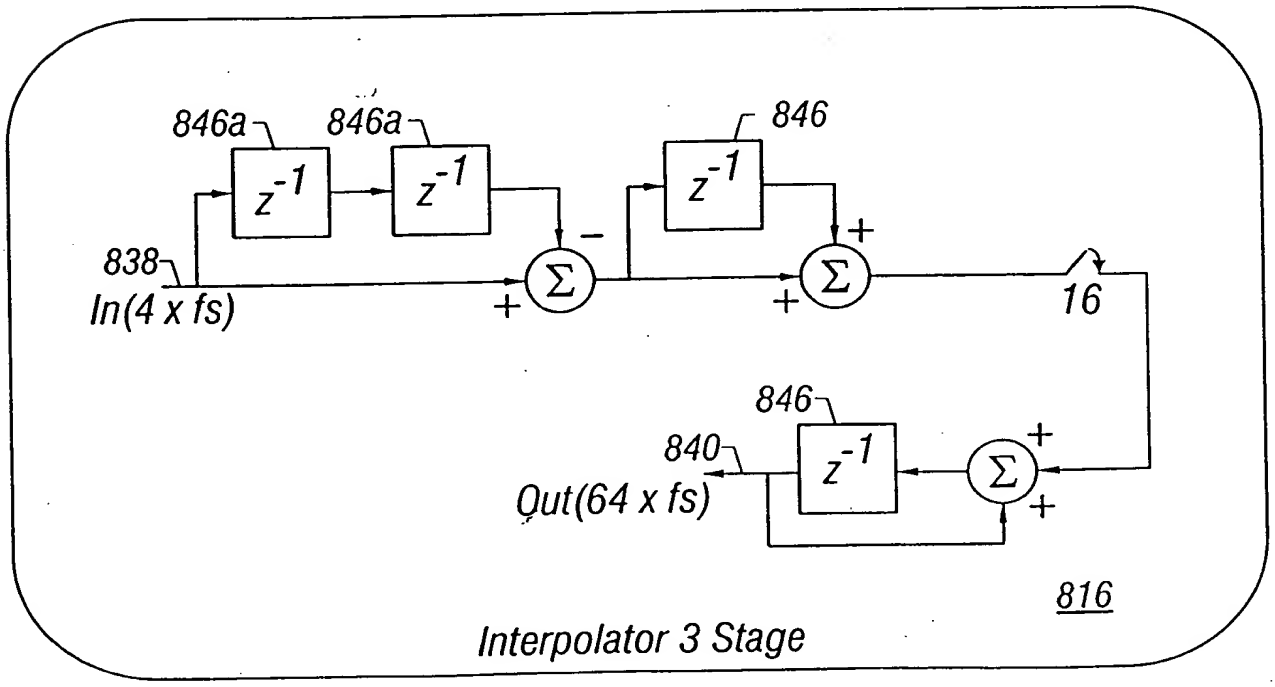


FIG. 61

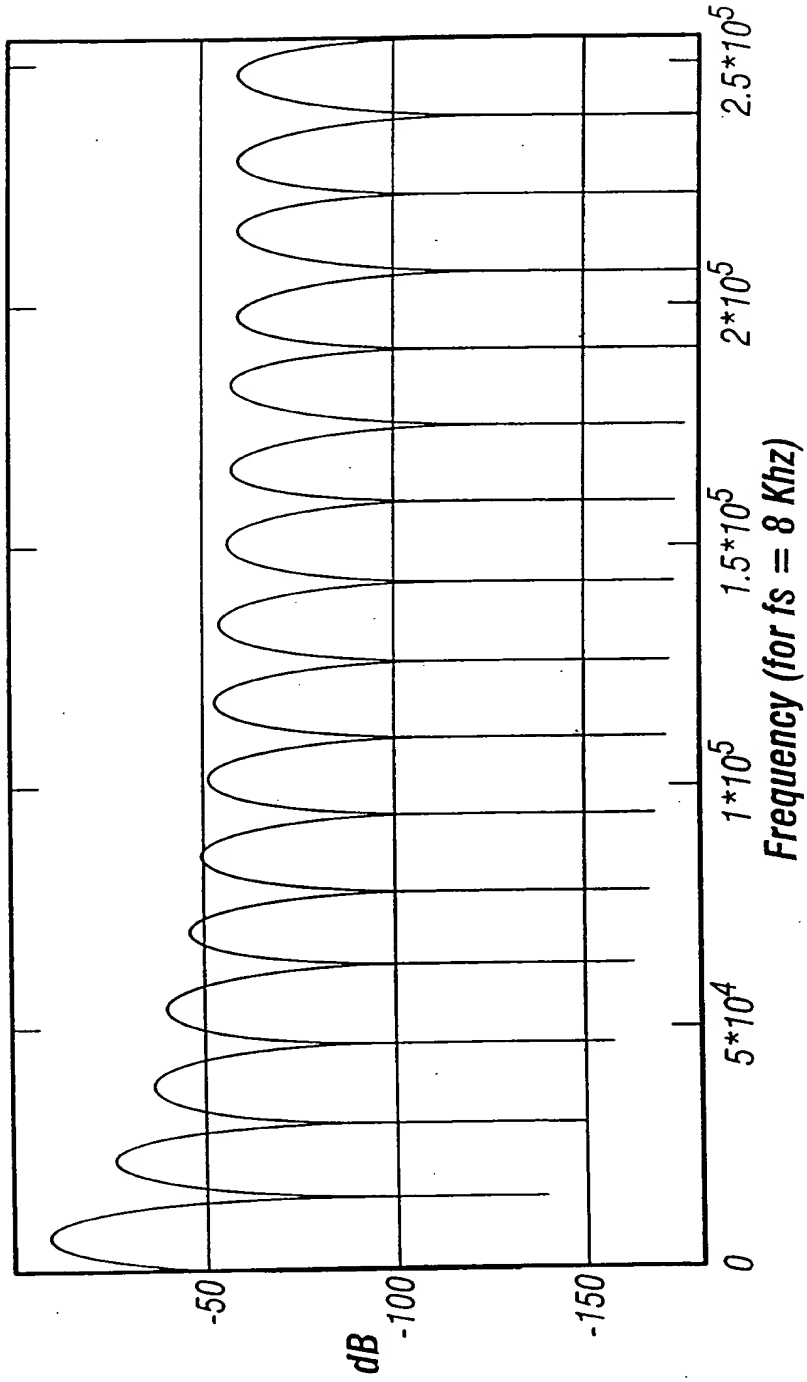

-50
-100
-150
dB
0
5*10^4
1*10^5
1.5*10^5
2*10^5
2.5*10^5
Frequency (for fs = 8 Khz)

FIG. 62A

REPLACEMENT SHEET

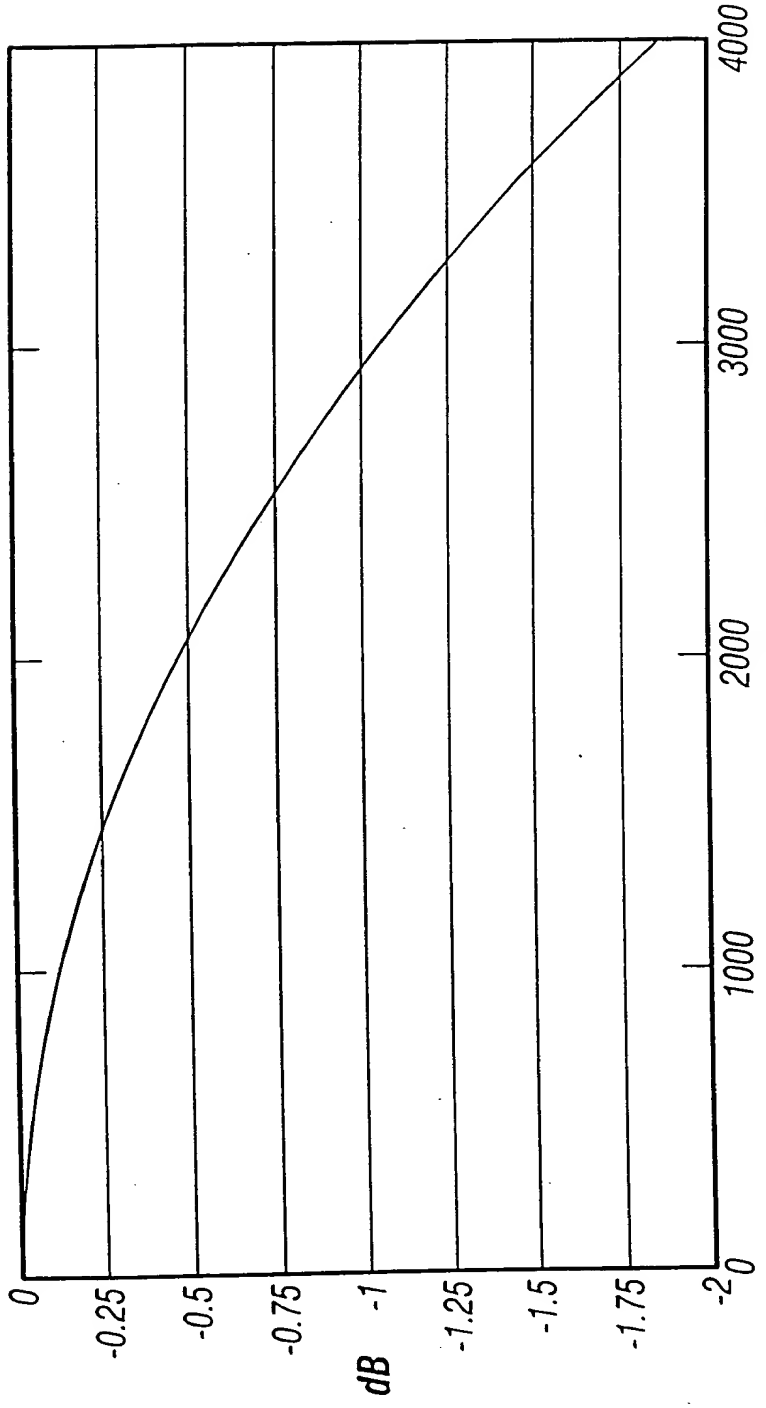


FIG. 62B

REPLACEMENT SHEET

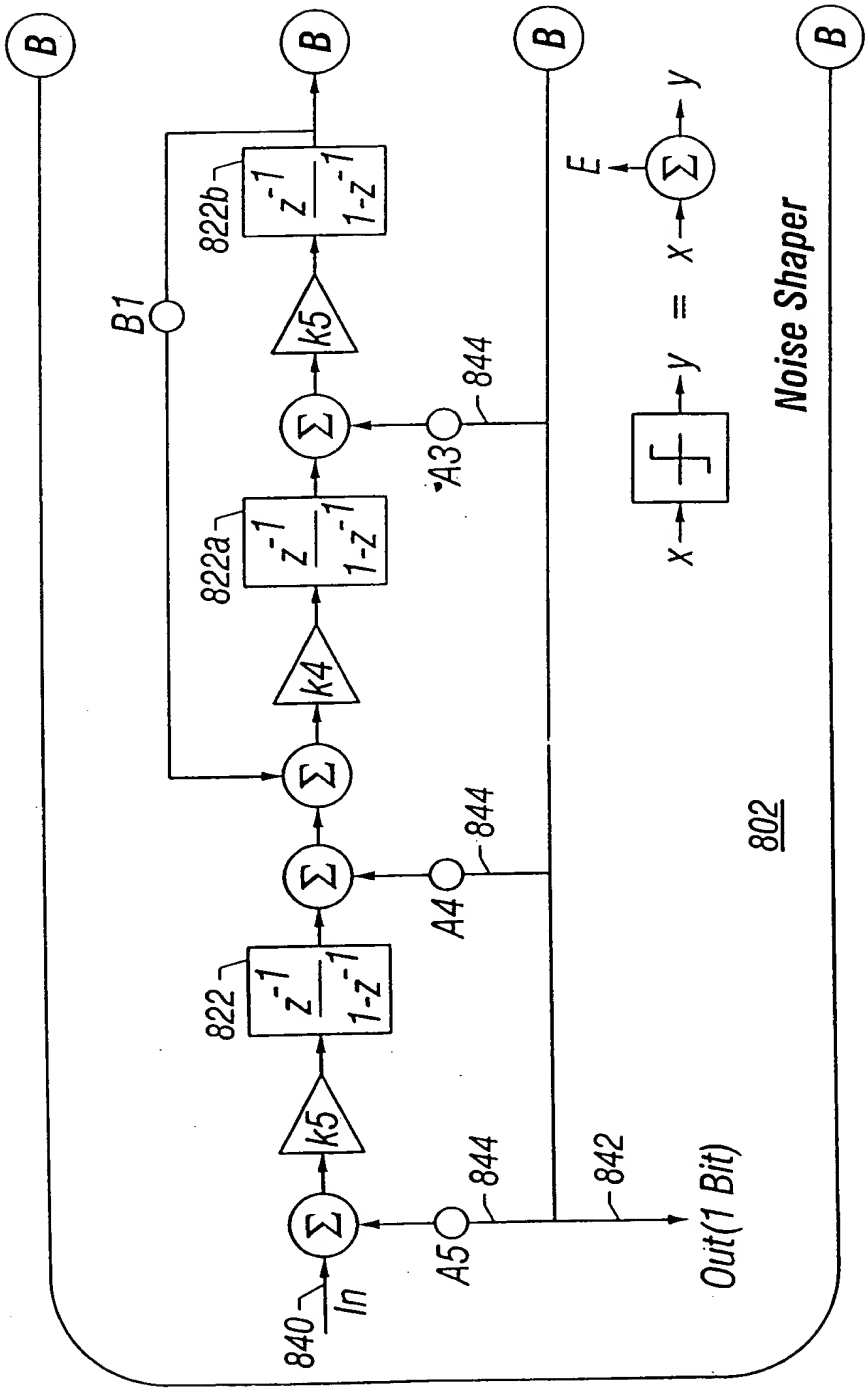


FIG. 63A

REPLACEMENT SHEET

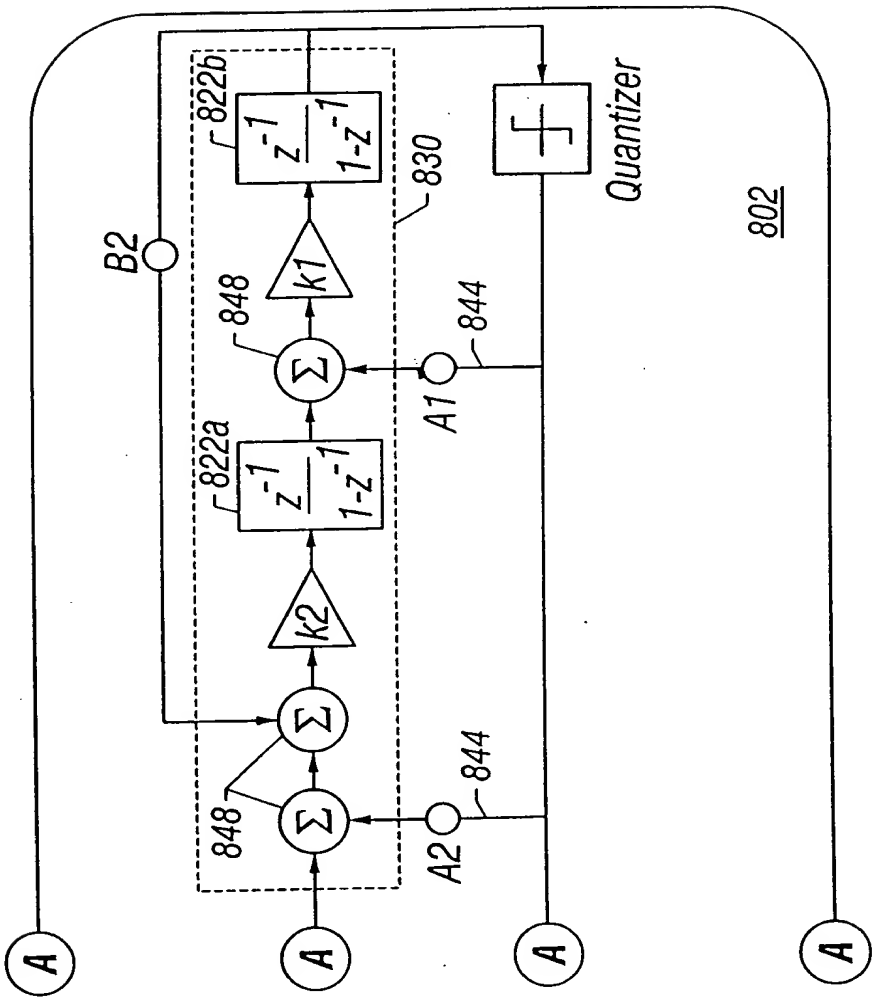


FIG. 63B

REPLACEMENT SHEET

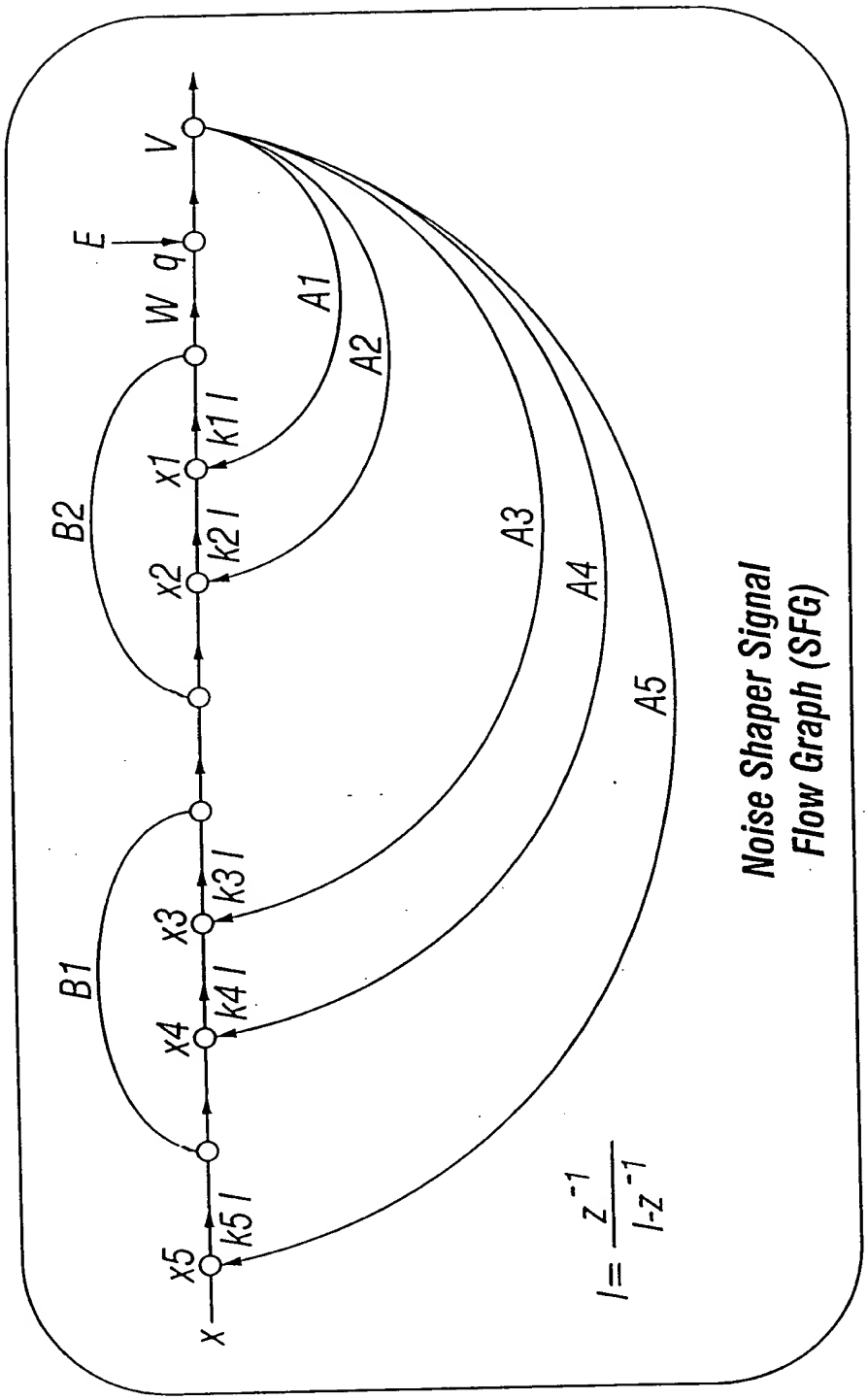


FIG. 64

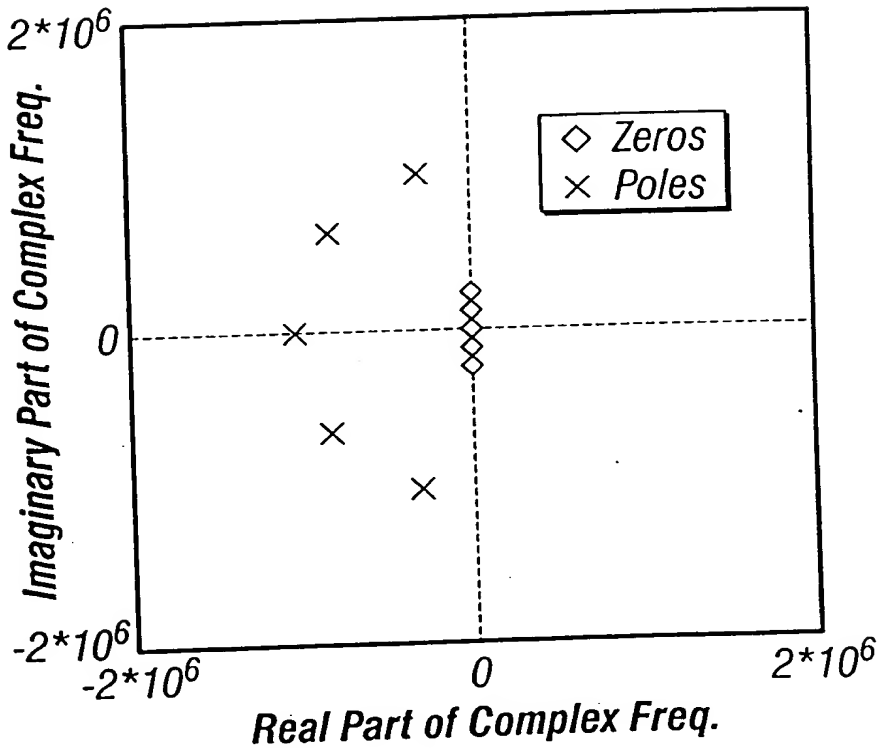

2*10^6
0
-2*10^6
-2*10^6
0
2*10^6
Imaginary Part of Complex Freq.
Real Part of Complex Freq.
Zeros
Poles

FIG. 65

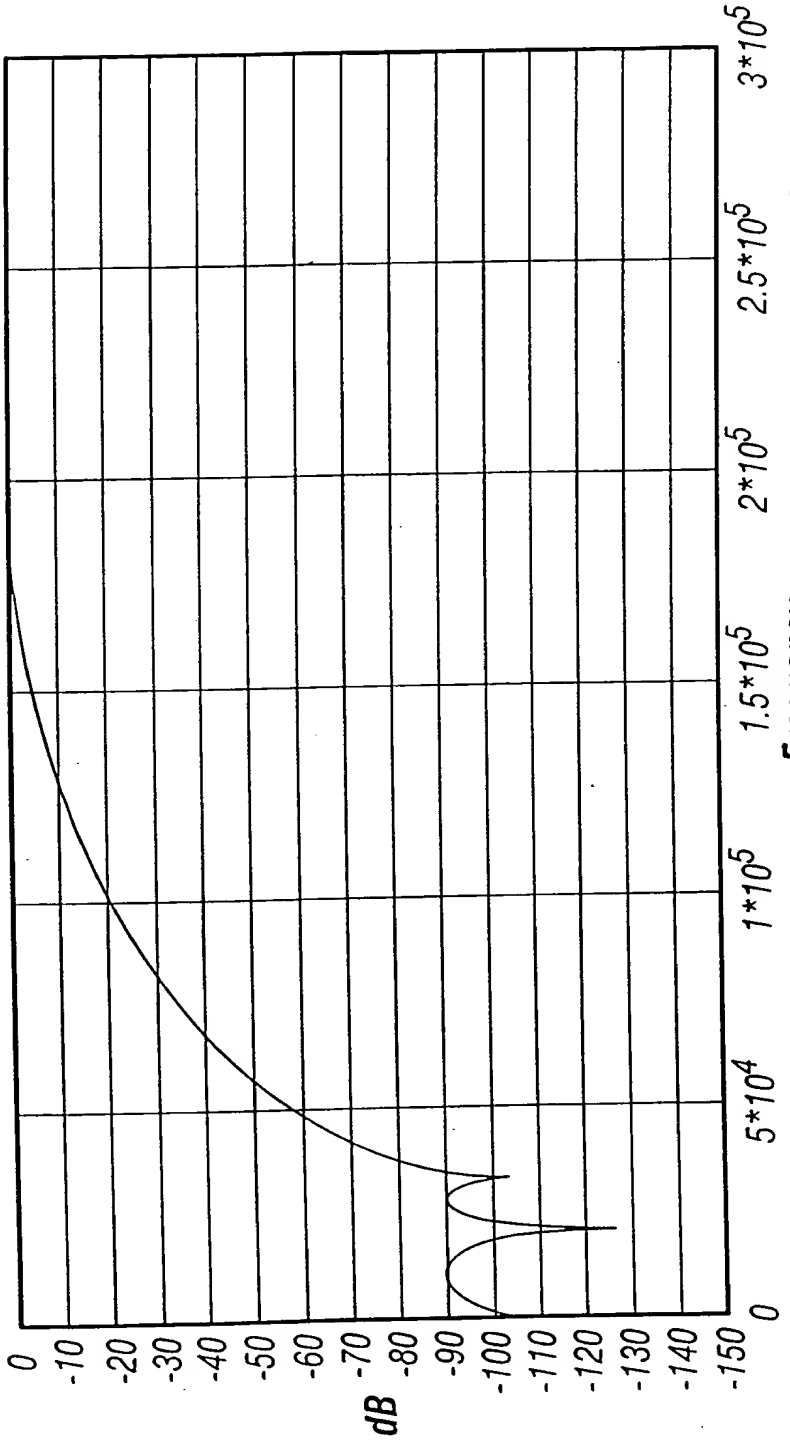

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
dB
0
5*10^4
1*10^5
1.5*10^5
2*10^5
2.5*10^5
3*10^5
Frequency

FIG. 66

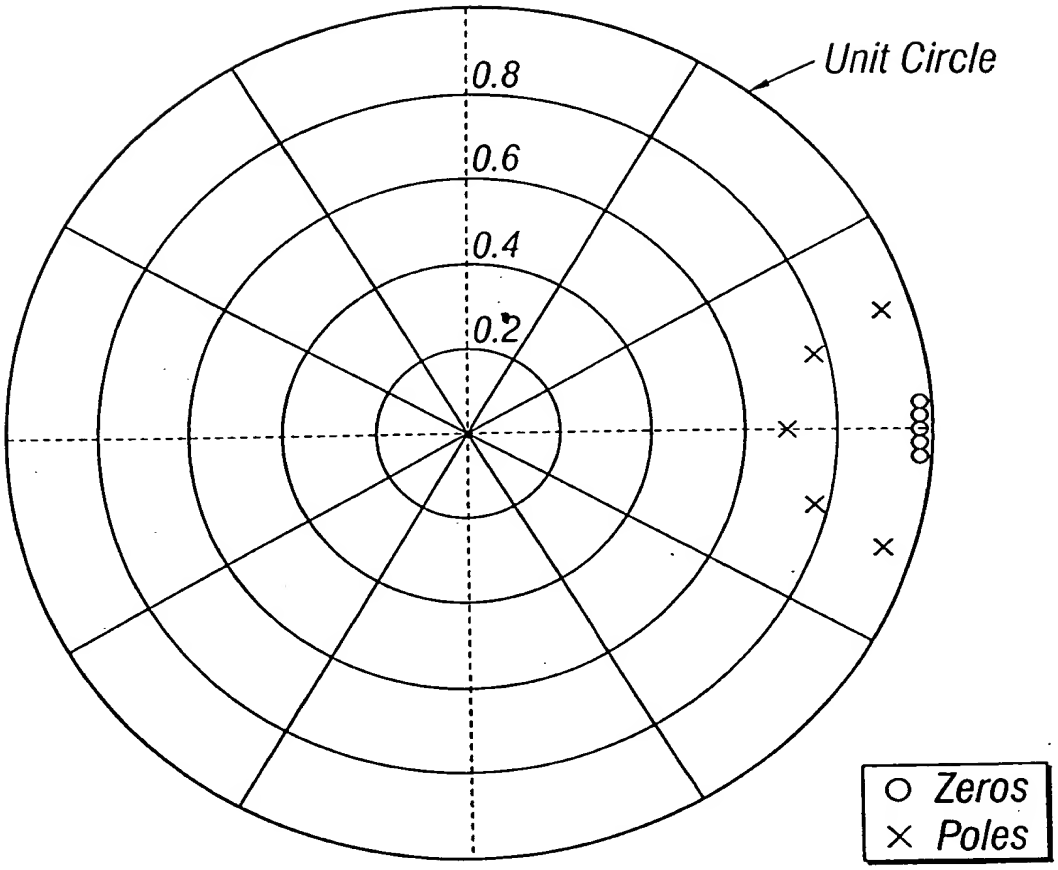


FIG. 67

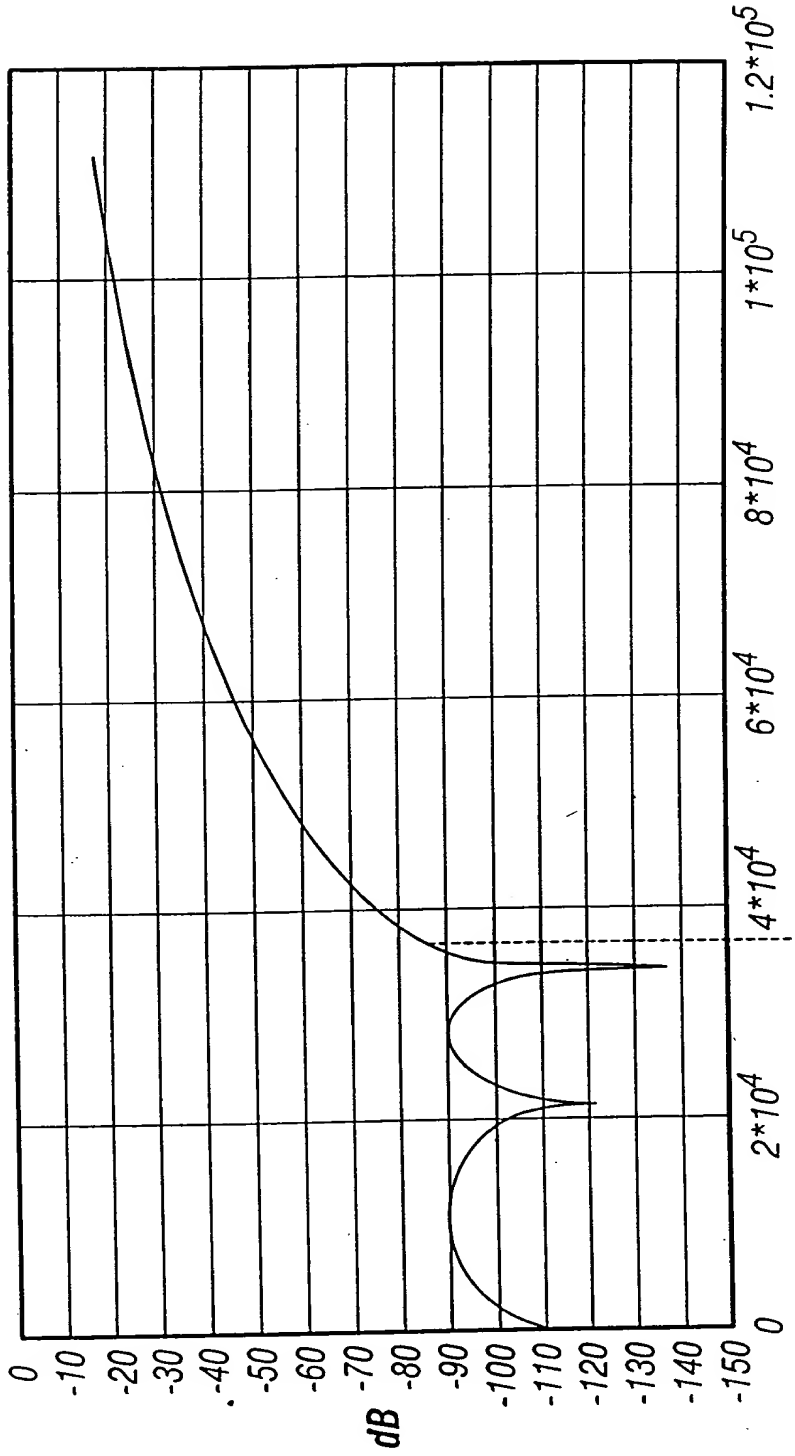

0
-10
-20
-30
-40
-50
-60
-70
-80
-90
-100
-110
-120
-130
-140
-150
dB
0
2*10^4
3.6*10^4
4*10^4
6*10^4
8*10^4
1*10^5
1.2*10^5
Frequency(Hz)
(fs = 48 Khz)

FIG. 68

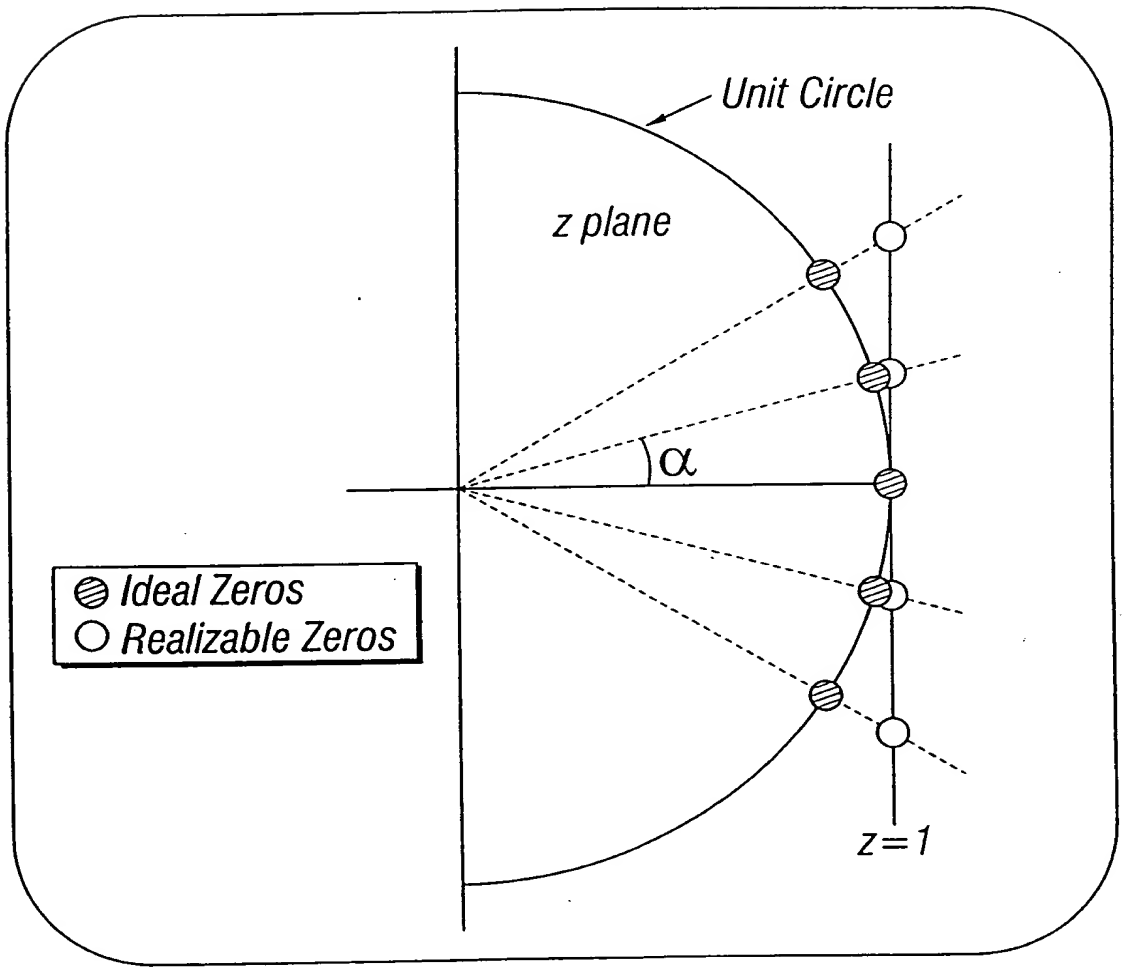


FIG. 69

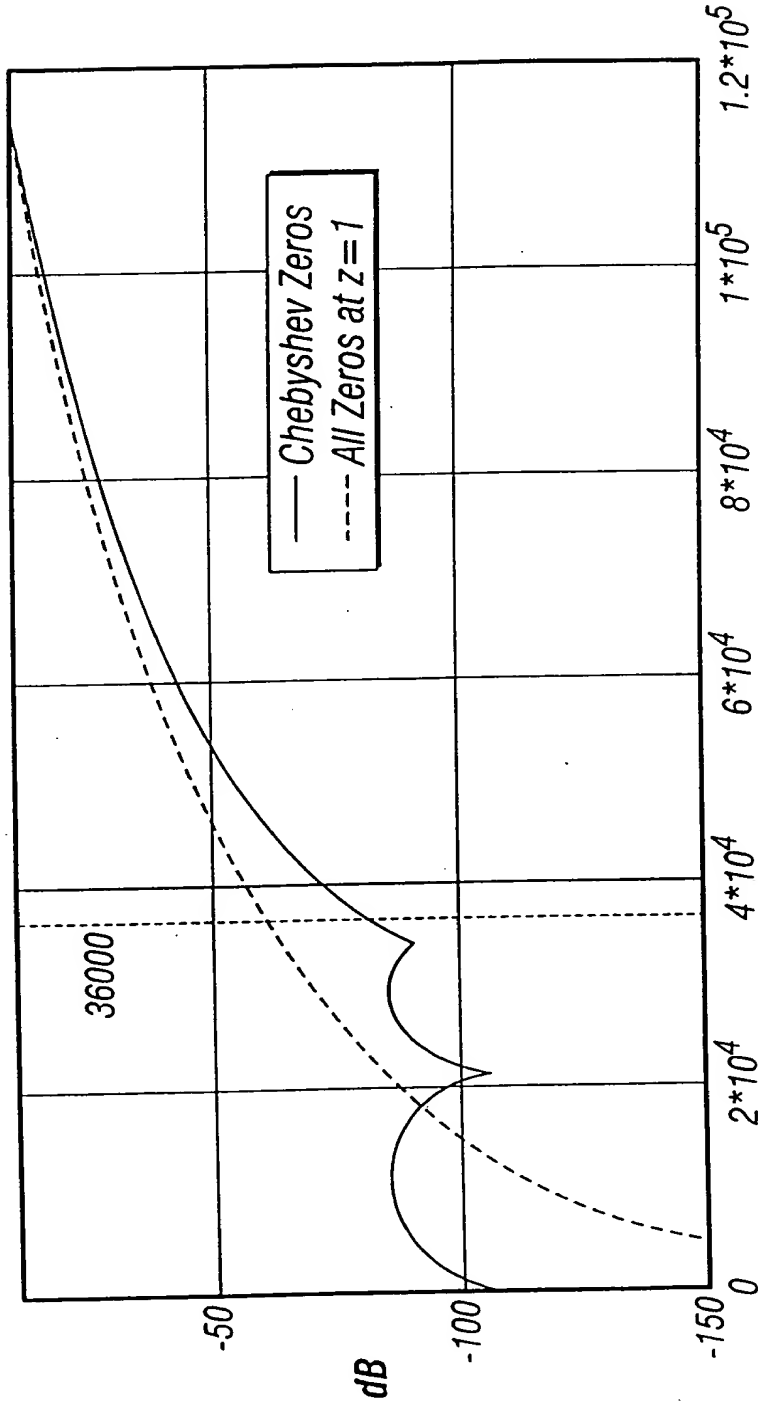

Chebyshev Zeros
All Zeros at z=1
36000
-50
-100
-150
dB
0
2*10^4
4*10^4
6*10^4
8*10^4
1*10^5
1.2*10^5
Frequency

FIG. 70

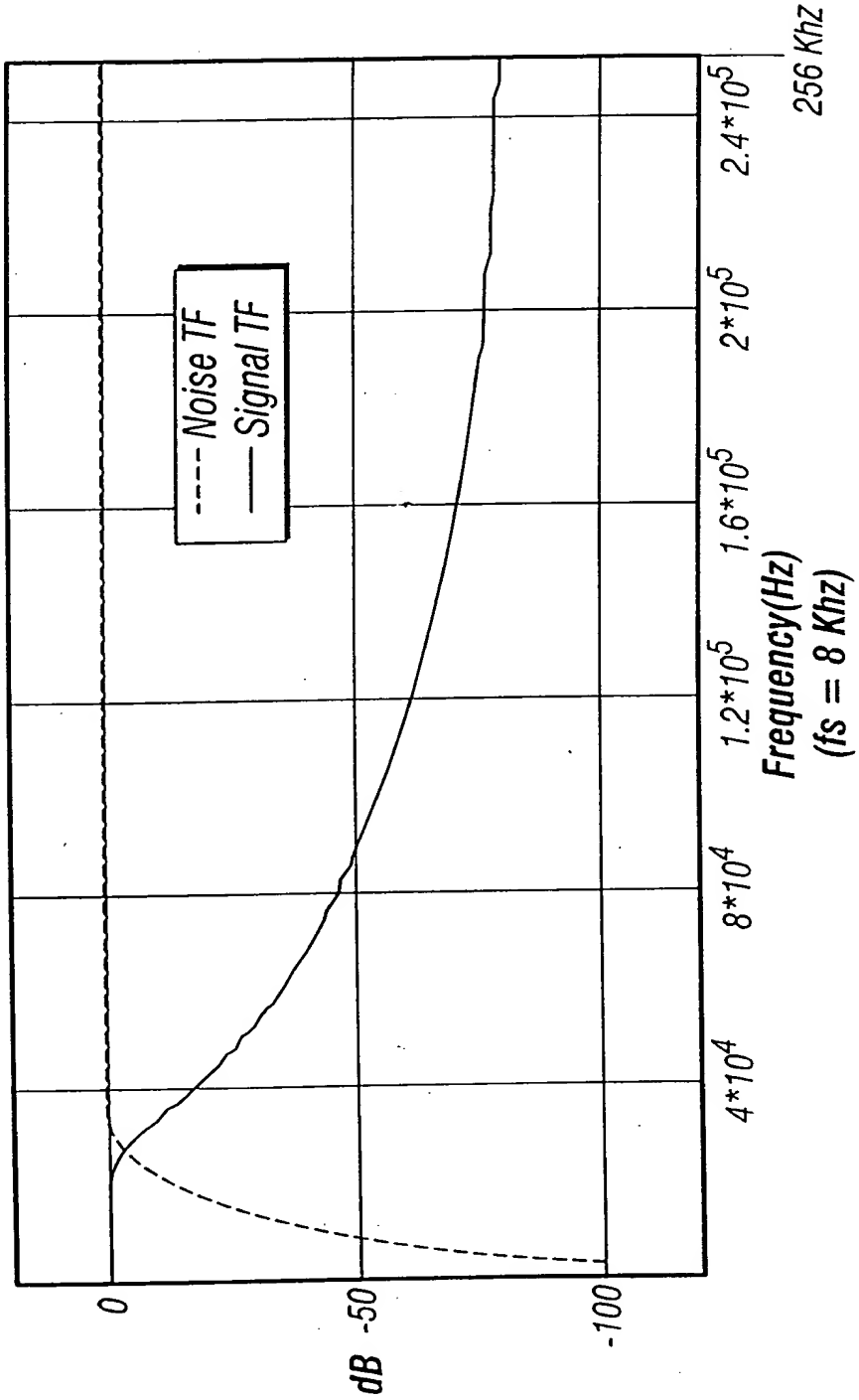

Noise TF
Signal TF
dB
0
-50
-100
Frequency(Hz)
(fs = 8 Khz)
4*10^4
8*10^4
1.2*10^5
1.6*10^5
2*10^5
2.4*10^5
256 Khz

FIG. 71

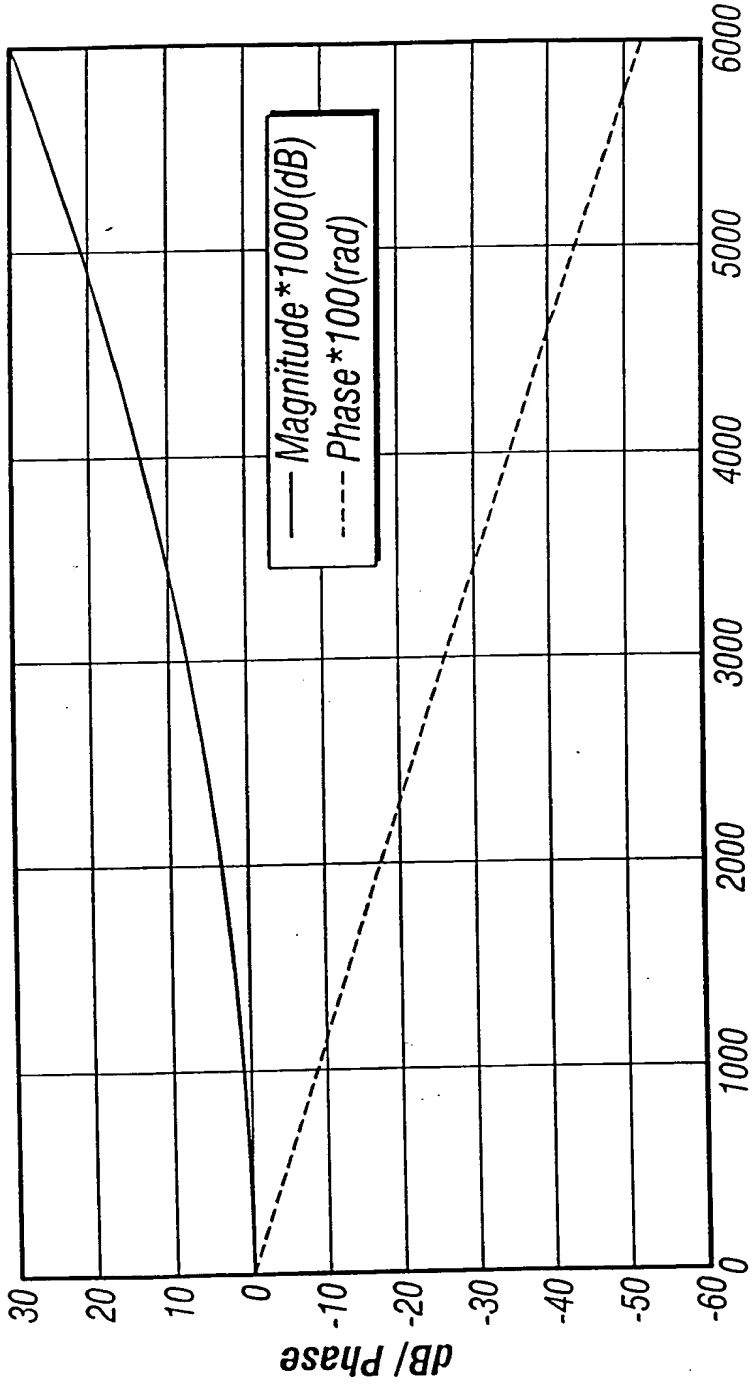

Magnitude*1000(dB)
Phase*100(rad)
dB/ Phase
30
20
10
0
-10
-20
-30
-40
-50
-60
0
1000
2000
3000
4000
5000
6000
Frequency(Hz)
(fs = 8 Khz)

FIG. 72

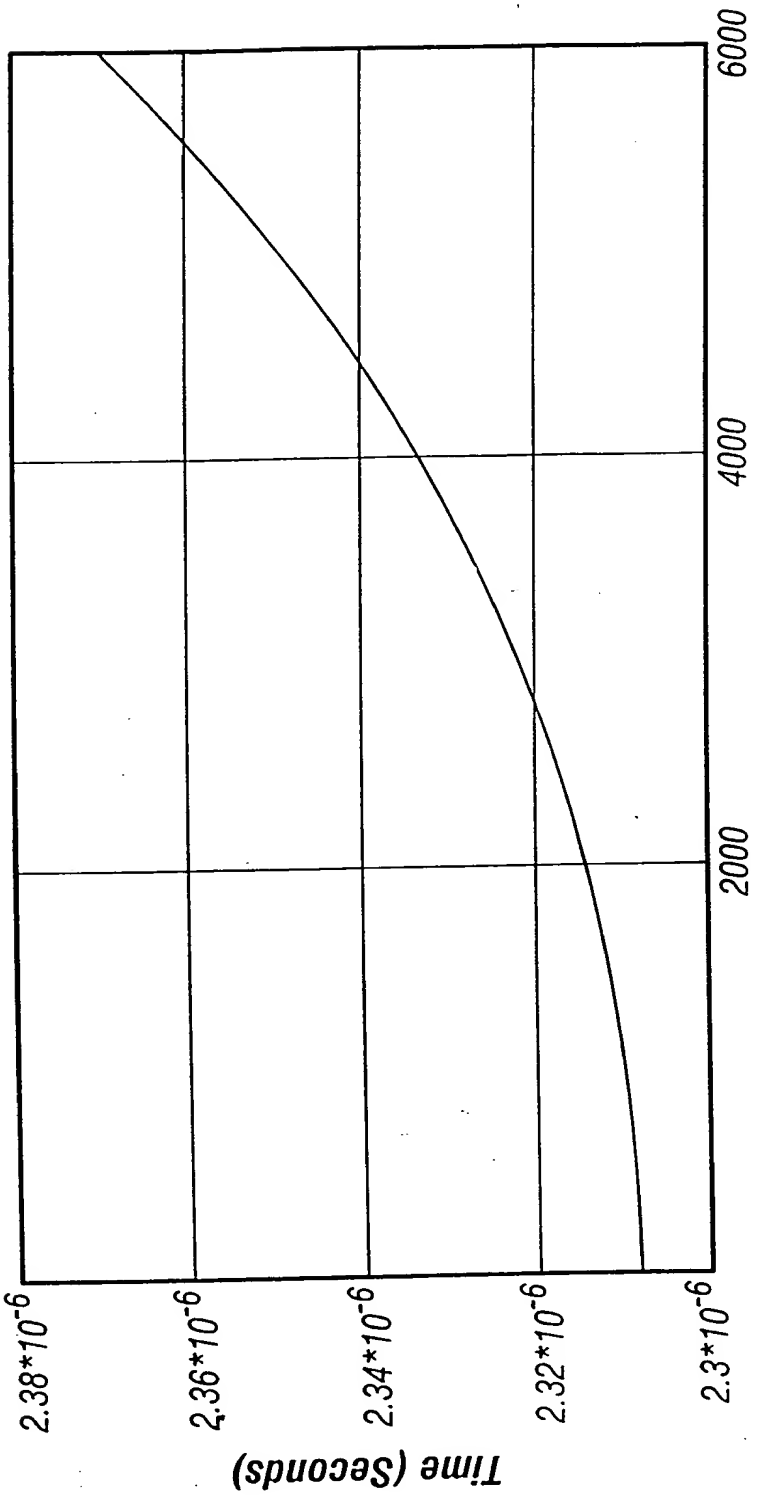

6000
4000
2000
2.38*10^-6
2.36*10^-6
2.34*10^-6
2.32*10^-6
2.3*10^-6
Time (Seconds)
Frequency(Hz)
(fs = 8 Khz)

FIG. 73

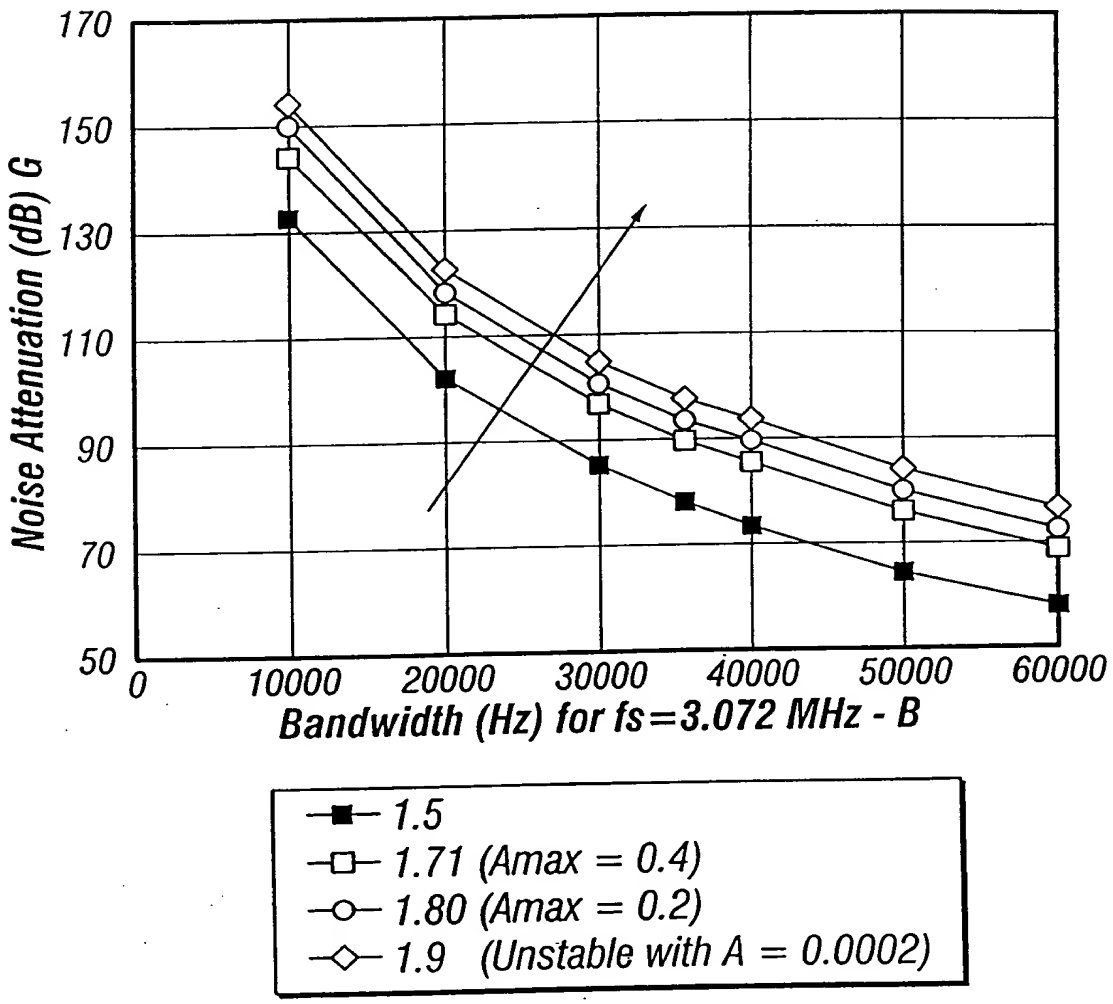

170
150
130
110
90
70
50
Noise Attenuation (dB) G
0
10000
20000
30000
40000
50000
60000
Bandwidth (Hz) for fs=3.072 MHz - B
1.5
1.71 (Amax = 0.4)
1.80 (Amax = 0.2)
1.9 (Unstable with A = 0.0002)

FIG. 74

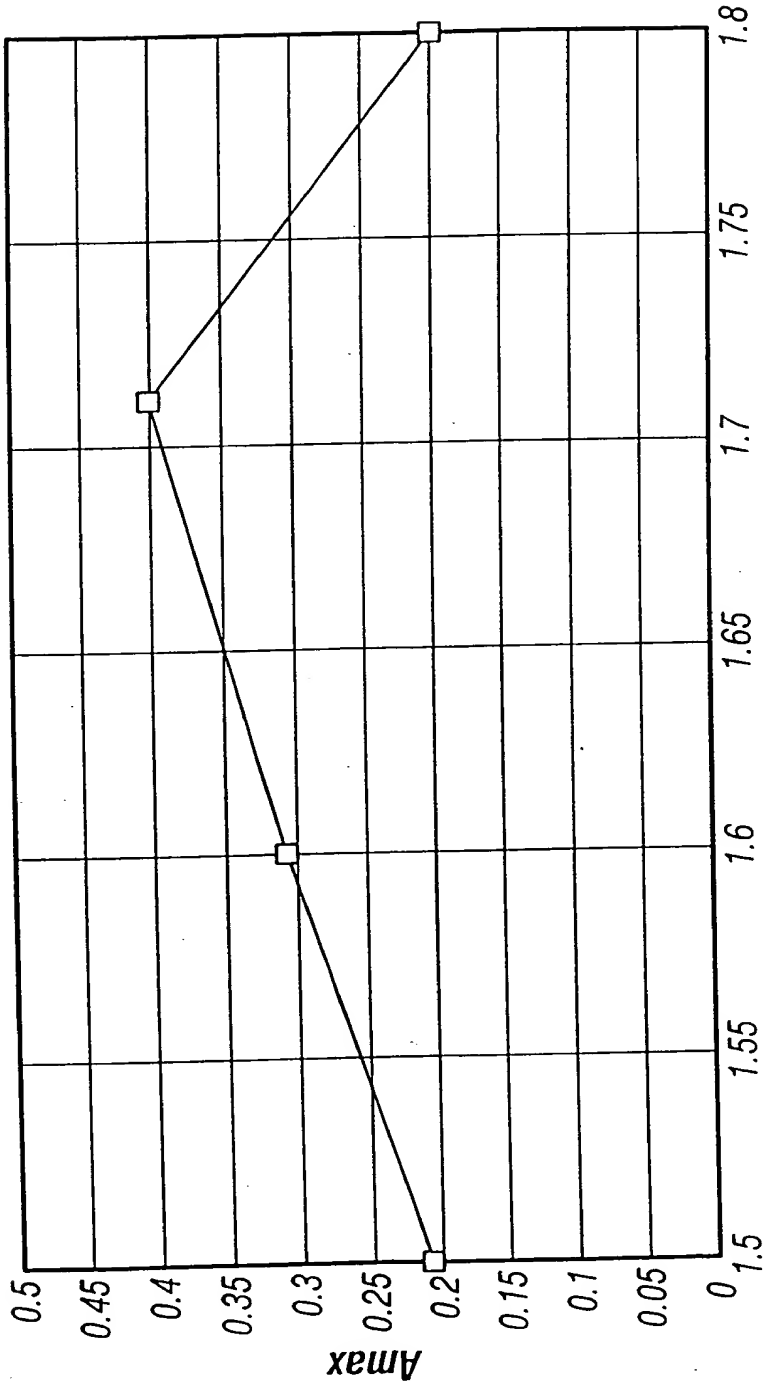


FIG. 75

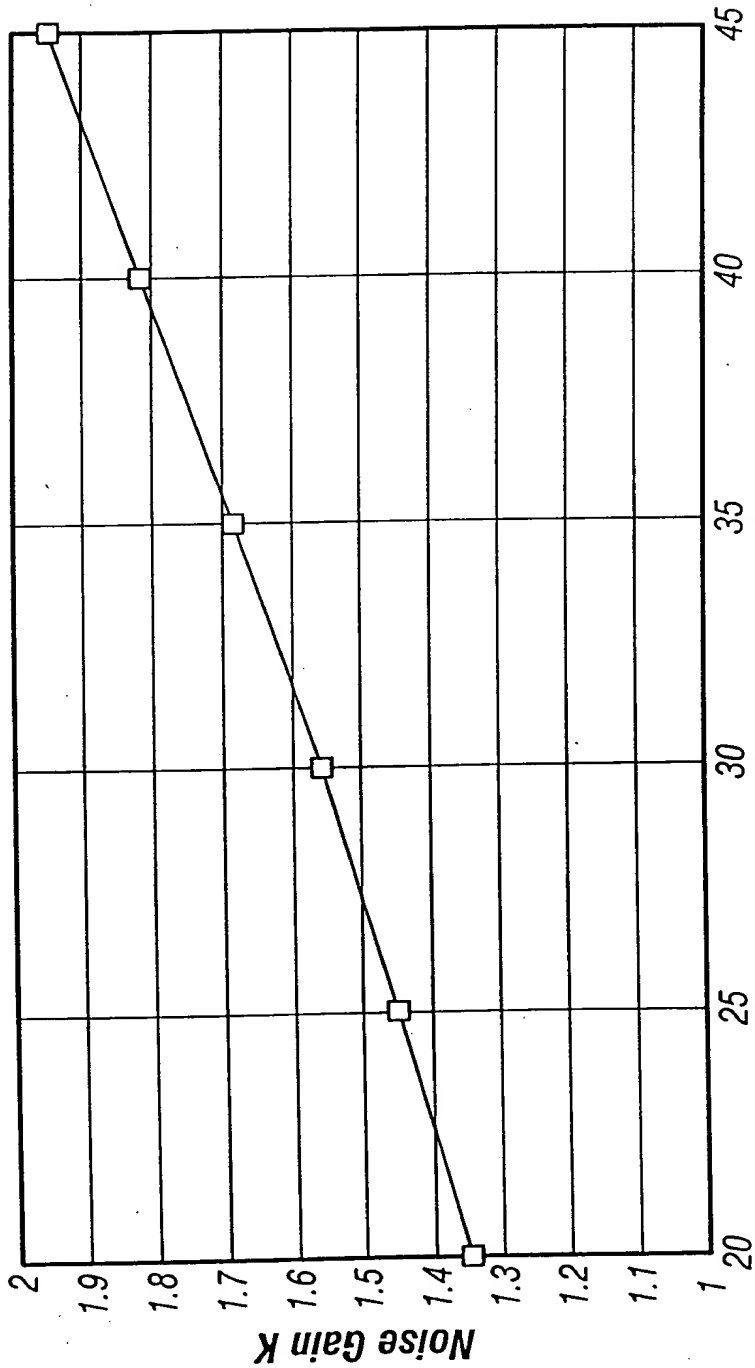

Noise Gain K
2
1.9
1.8
1.7
1.6
1.5
1.4
1.3
1.2
1.1
1
Bandwidth (KHz)
20
25
30
35
40
45

FIG. 76

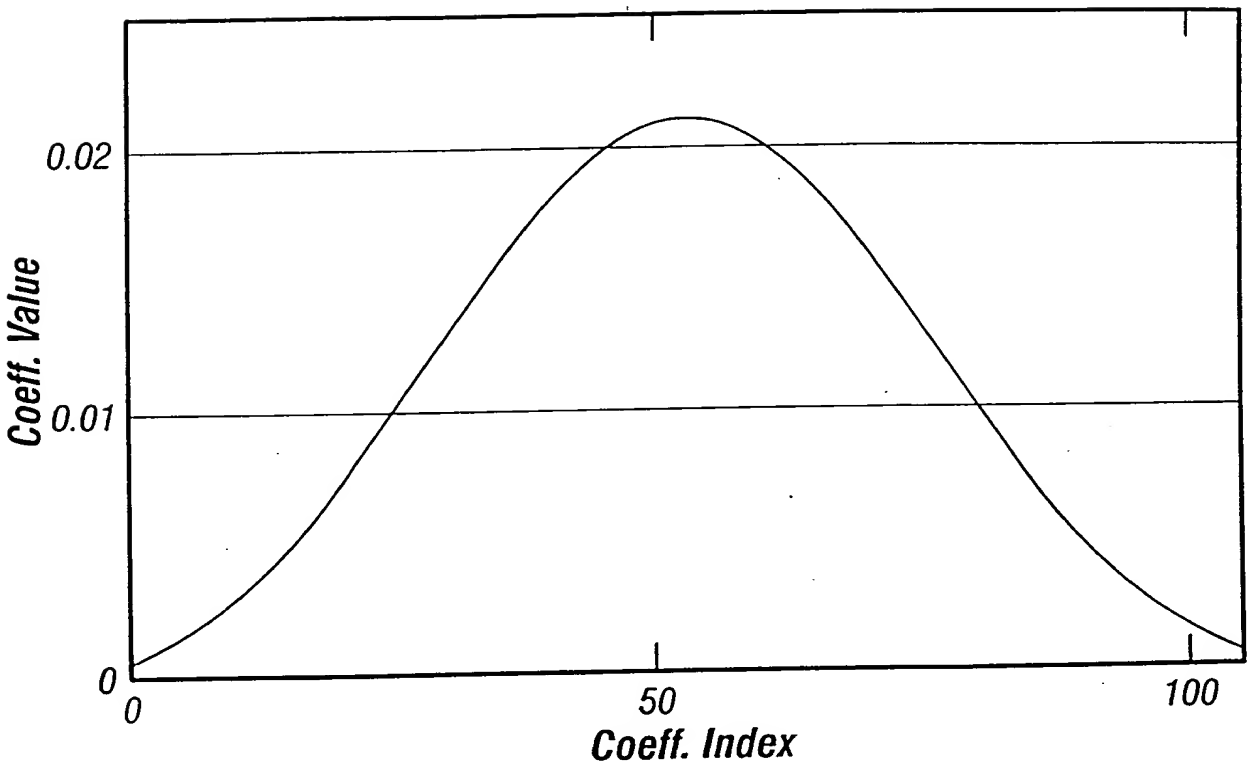


FIG. 77

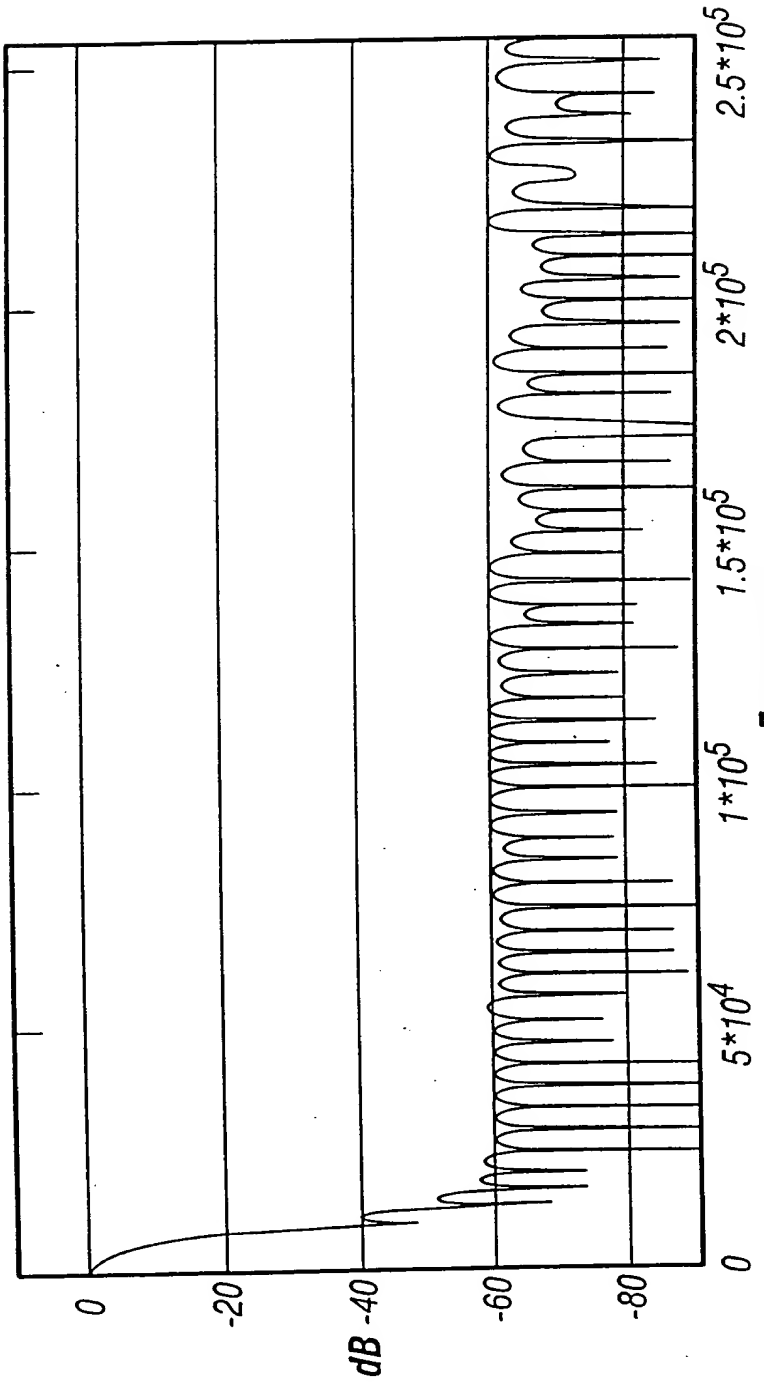


FIG. 78

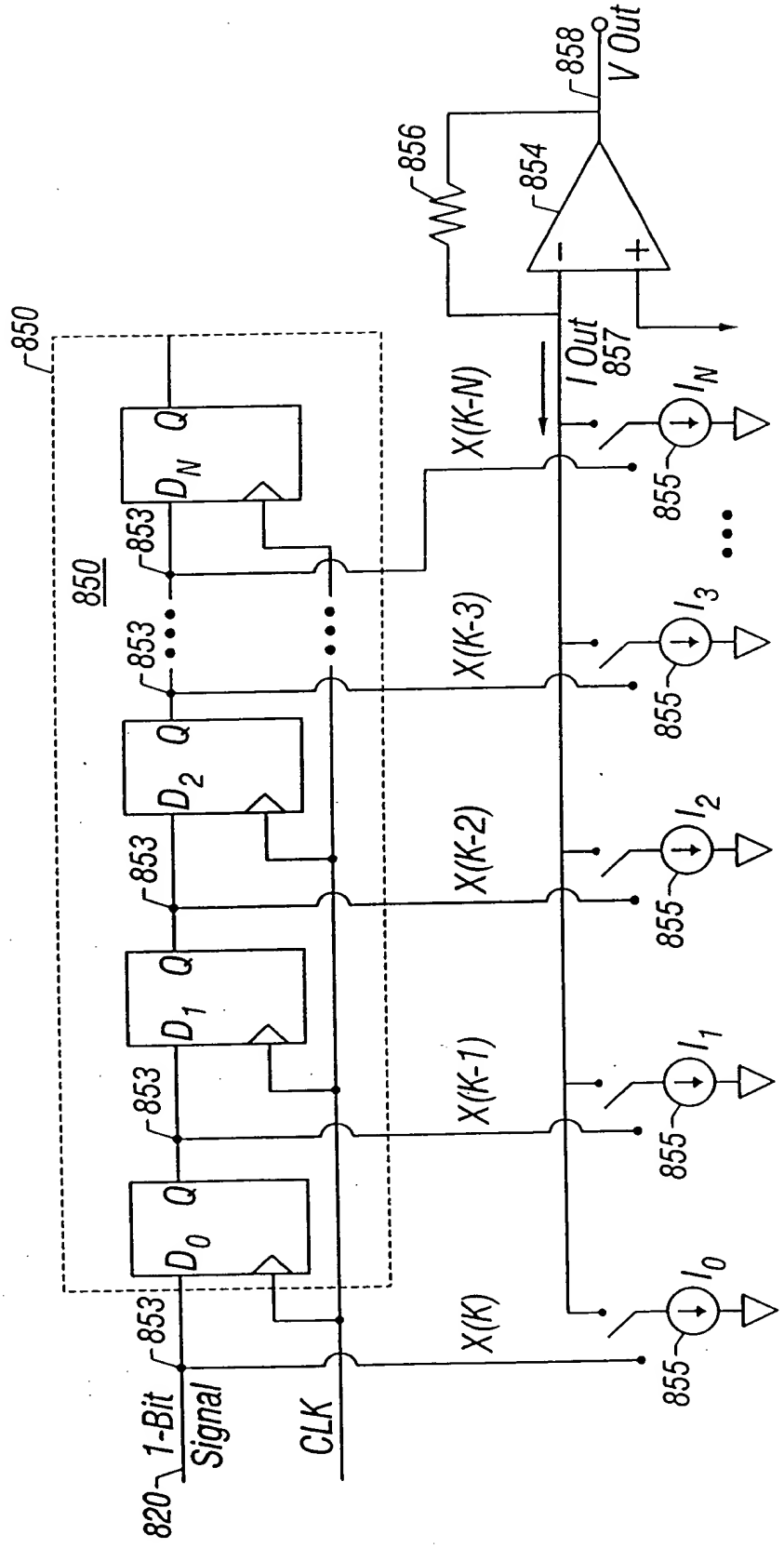

850
858
V Out
856
854
I Out
857
X(K-N)
X(K-3)
X(K-2)
X(K-1)
X(K)
I_N
I_3
I_2
I_1
I_0
855
D_N
D_2
D_1
D_0
Q
853
1-Bit
Signal
820
CLK

FIG. 79

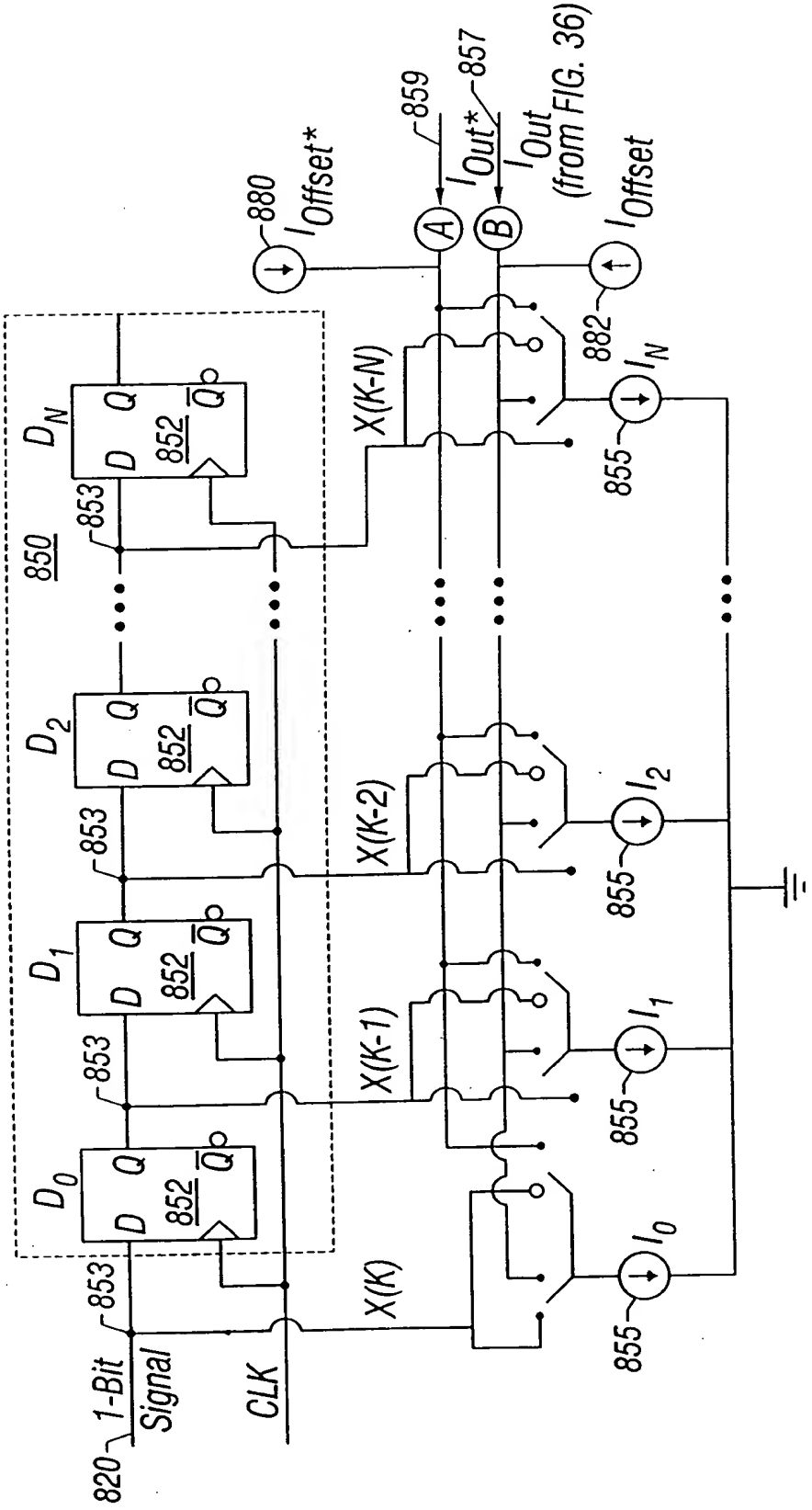

880
I_{Offset}*
859
A
I_{Out}*
857
B
I_{Out} (from FIG. 36)
I_{Offset}
882
I_N
855
X(K-N)
D_N
Q
D
852
$\overline{Q}$
853
850
D_2
X(K-2)
I_2
D_1
X(K-1)
I_1
D_0
X(K)
I_0
820
1-Bit Signal
CLK

FIG. 80

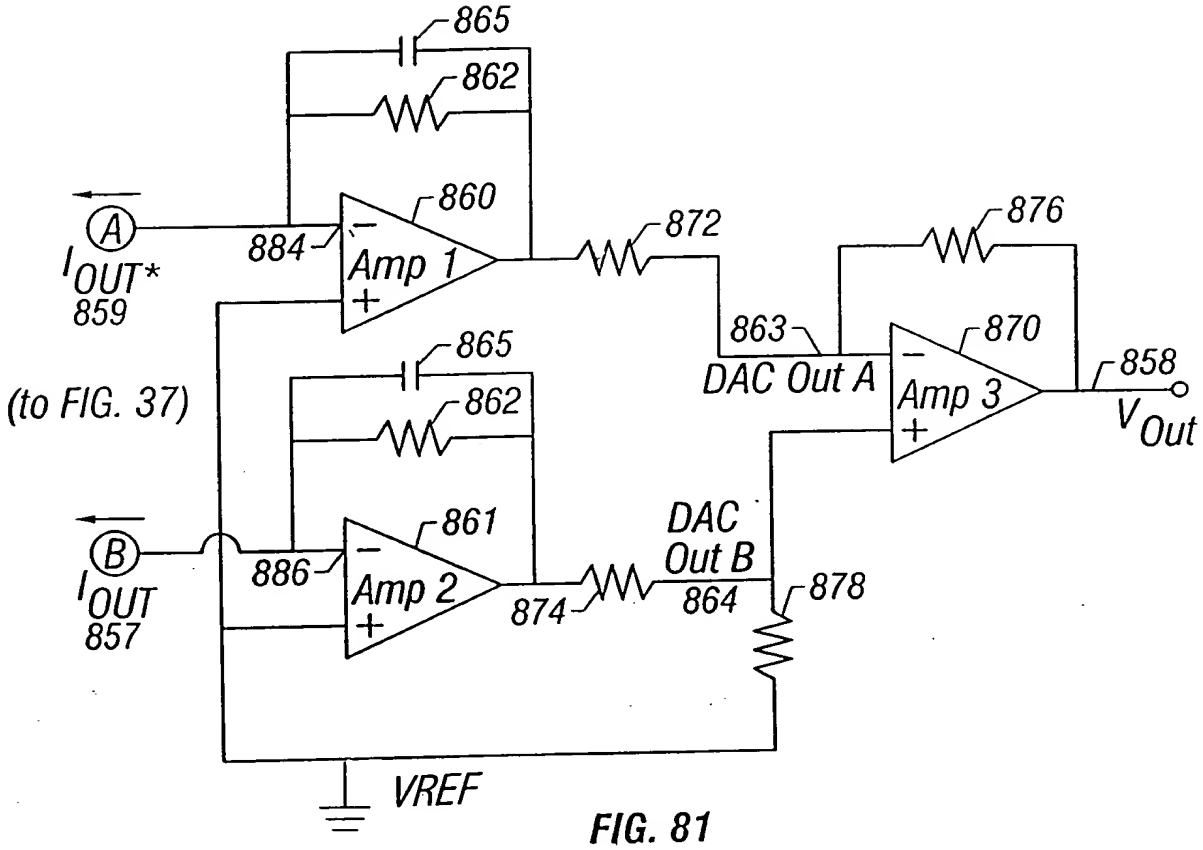

865
862
860
872
876
A
I_{OUT}*
859
884
Amp 1
863
DAC Out A
870
Amp 3
858
V_{Out}
(to FIG. 37)
865
862
861
B
I_{OUT}
857
886
Amp 2
874
DAC
Out B
864
878
VREF

FIG. 81

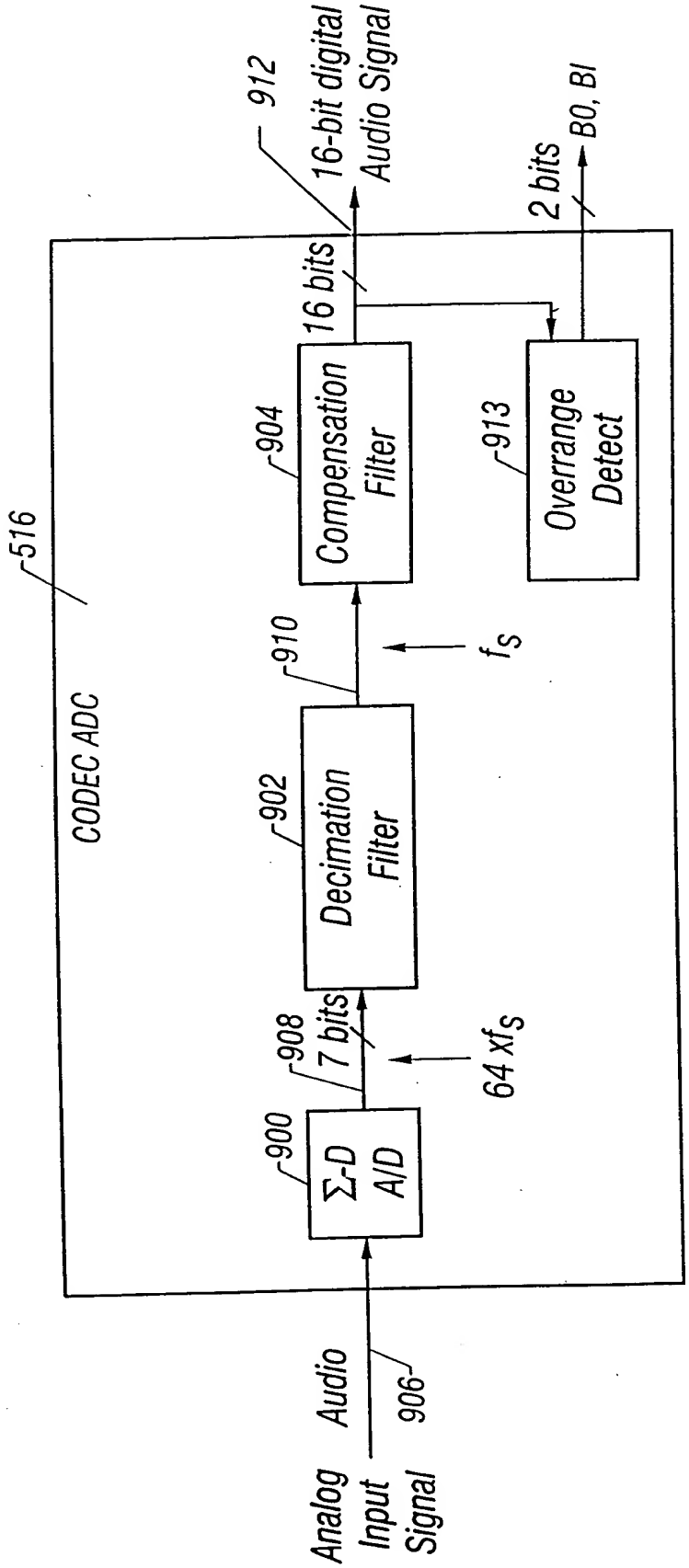

Analog Input Signal
Audio
906
CODEC ADC
516
Σ-D A/D
900
7 bits
908
64 xfS
Decimation Filter
902
910
fS
Compensation Filter
904
16 bits
Overrange Detect
913
2 bits
B0, BI
912
16-bit digital Audio Signal

FIG. 82

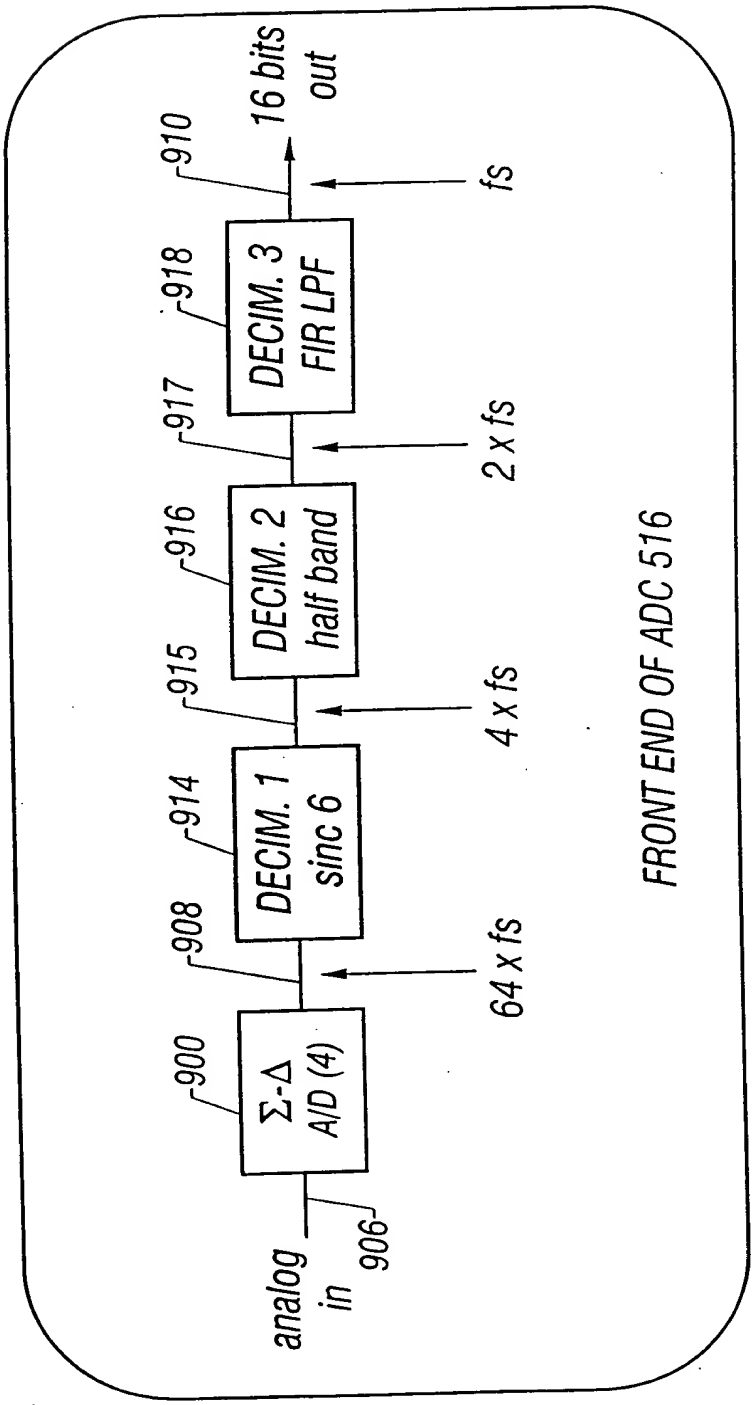

FRONT END OF ADC 516
analog in
906
Σ-Δ A/D (4)
900
908
64 x fs
DECIM. 1 sinc 6
914
915
4 x fs
DECIM. 2 half band
916
917
2 x fs
DECIM. 3 FIR LPF
918
910
fs
16 bits out

FIG. 83

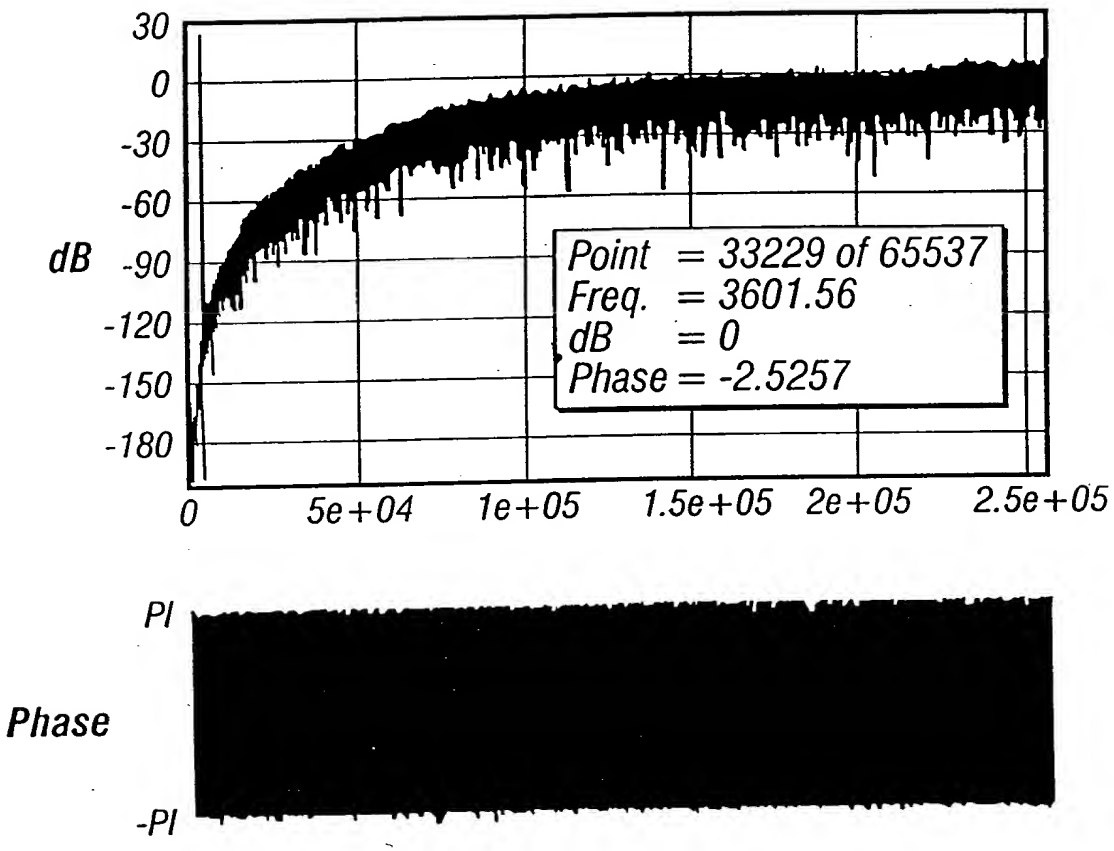

30
0
-30
-60
dB -90
-120
-150
-180
0
5e+04
1e+05
1.5e+05
2e+05
2.5e+05
Point = 33229 of 65537
Freq. = 3601.56
dB = 0
Phase = -2.5257
PI
Phase
-PI

FIG. 84

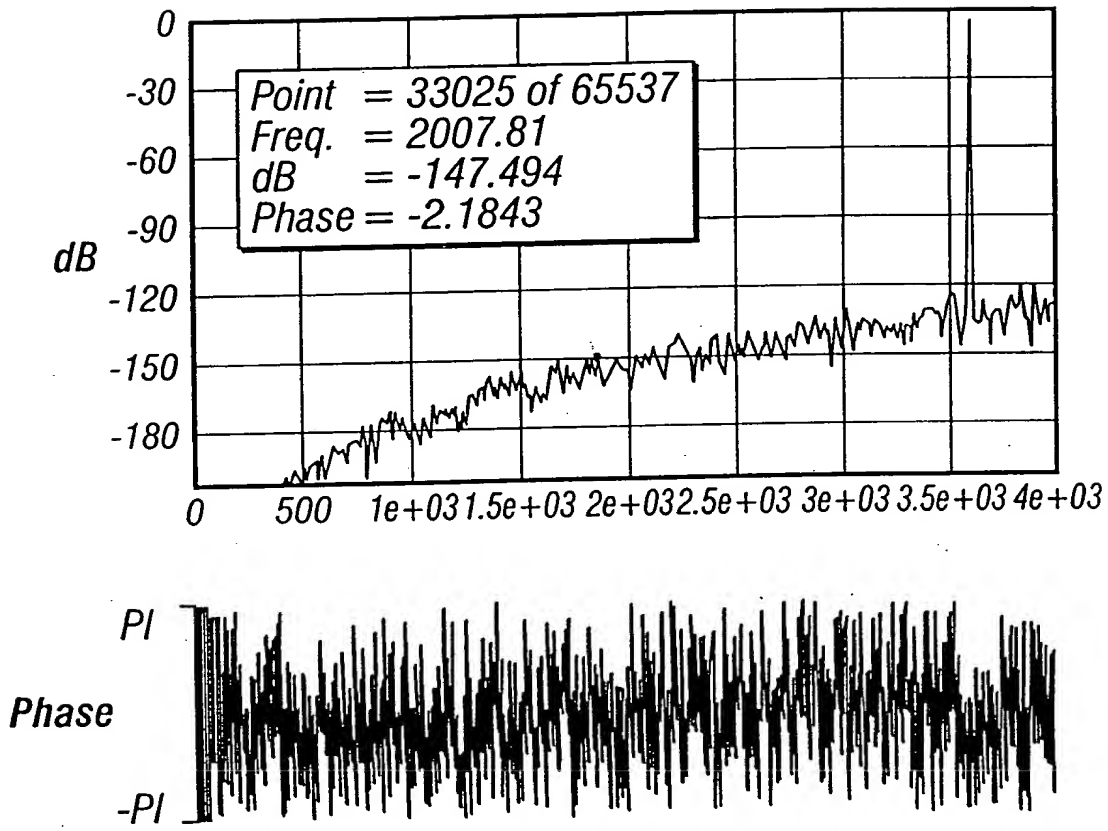

0
-30
-60
-90
-120
-150
-180
dB
Point = 33025 of 65537
Freq. = 2007.81
dB = -147.494
Phase = -2.1843
0
500
1e+03
1.5e+03
2e+03
2.5e+03
3e+03
3.5e+03
4e+03
PI
Phase
-PI

FIG. 85

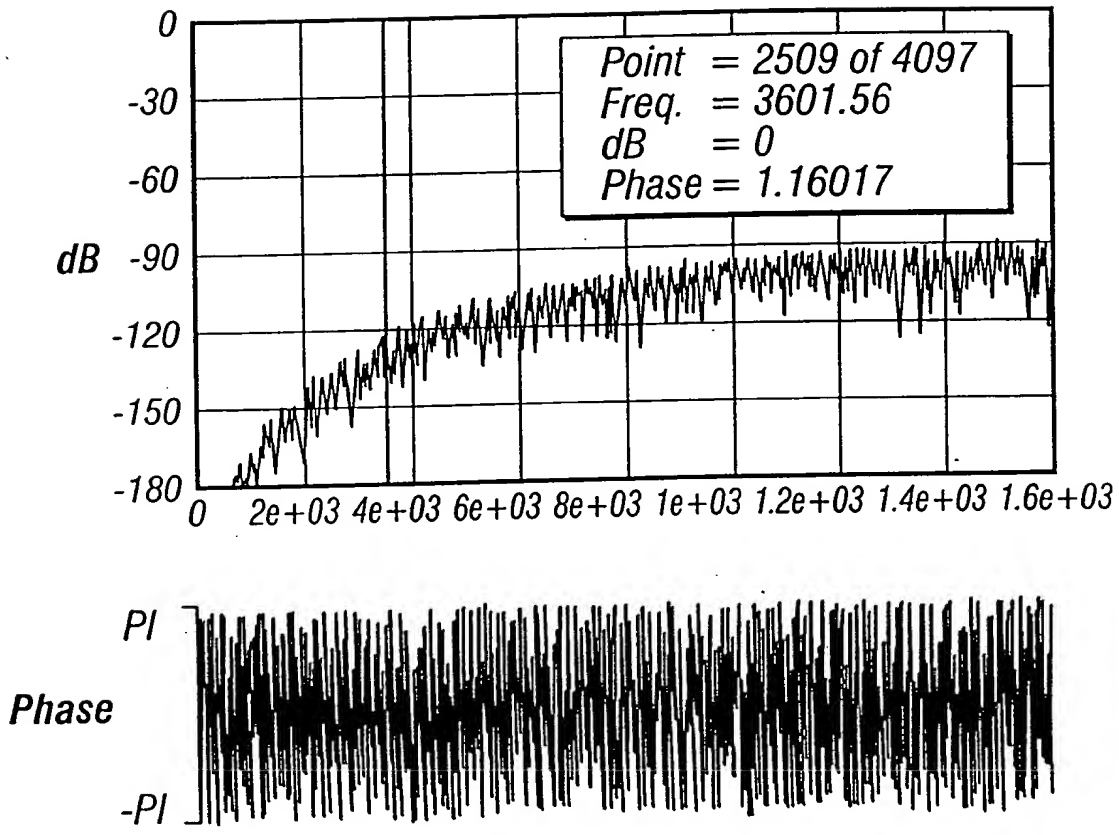

0
-30
-60
dB -90
-120
-150
-180
0
2e+03
4e+03
6e+03
8e+03
1e+03
1.2e+03
1.4e+03
1.6e+03
Point = 2509 of 4097
Freq. = 3601.56
dB = 0
Phase = 1.16017
PI
Phase
-PI

FIG. 86

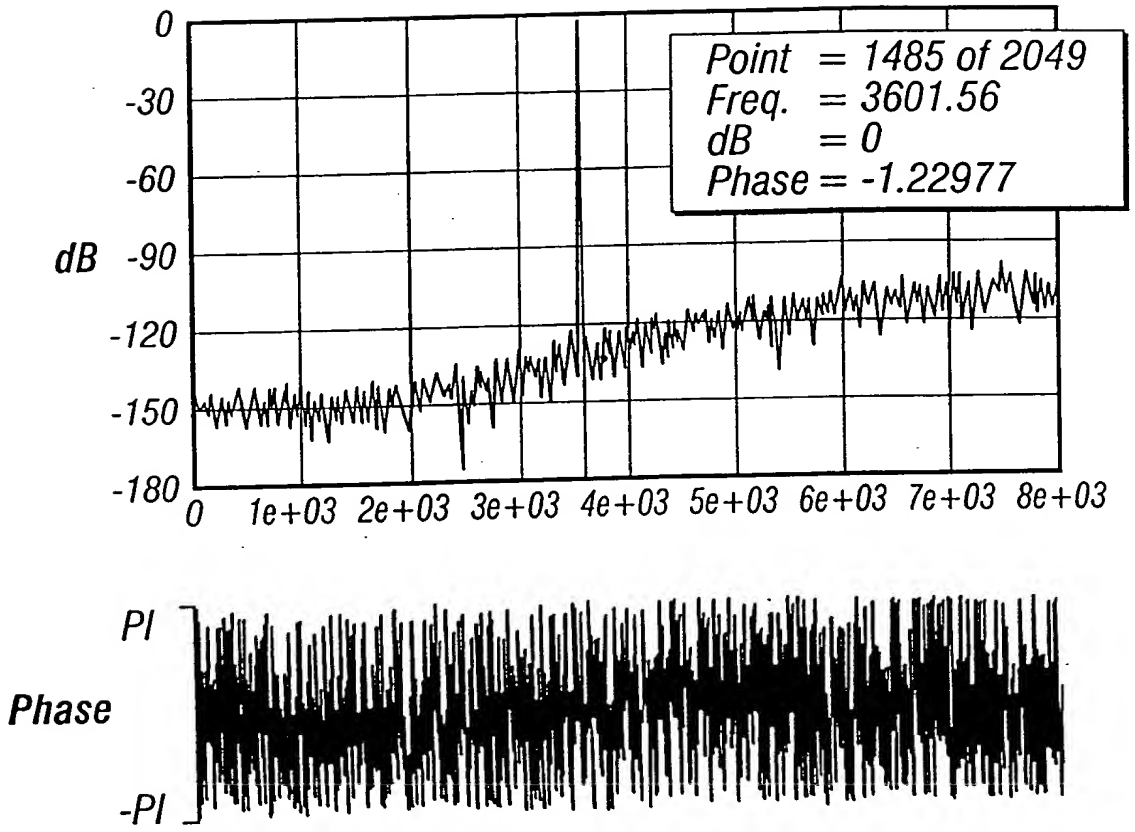

0
-30
-60
dB -90
-120
-150
-180
0
1e+03
2e+03
3e+03
4e+03
5e+03
6e+03
7e+03
8e+03
Point = 1485 of 2049
Freq. = 3601.56
dB = 0
Phase = -1.22977
PI
Phase
-PI

FIG. 87

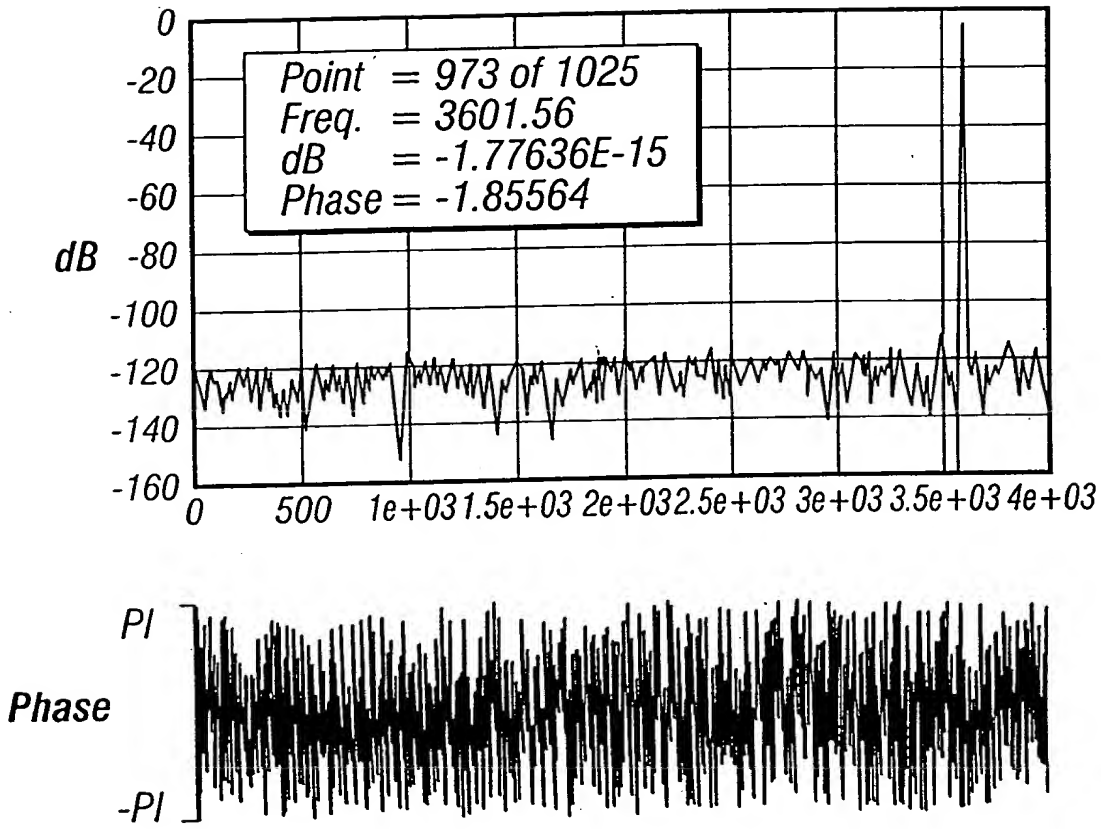

0
-20
-40
-60
-80
-100
-120
-140
-160
dB
Point = 973 of 1025
Freq. = 3601.56
dB = -1.77636E-15
Phase = -1.85564
0
500
1e+03
1.5e+03
2e+03
2.5e+03
3e+03
3.5e+03
4e+03
PI
-PI
Phase

FIG. 88

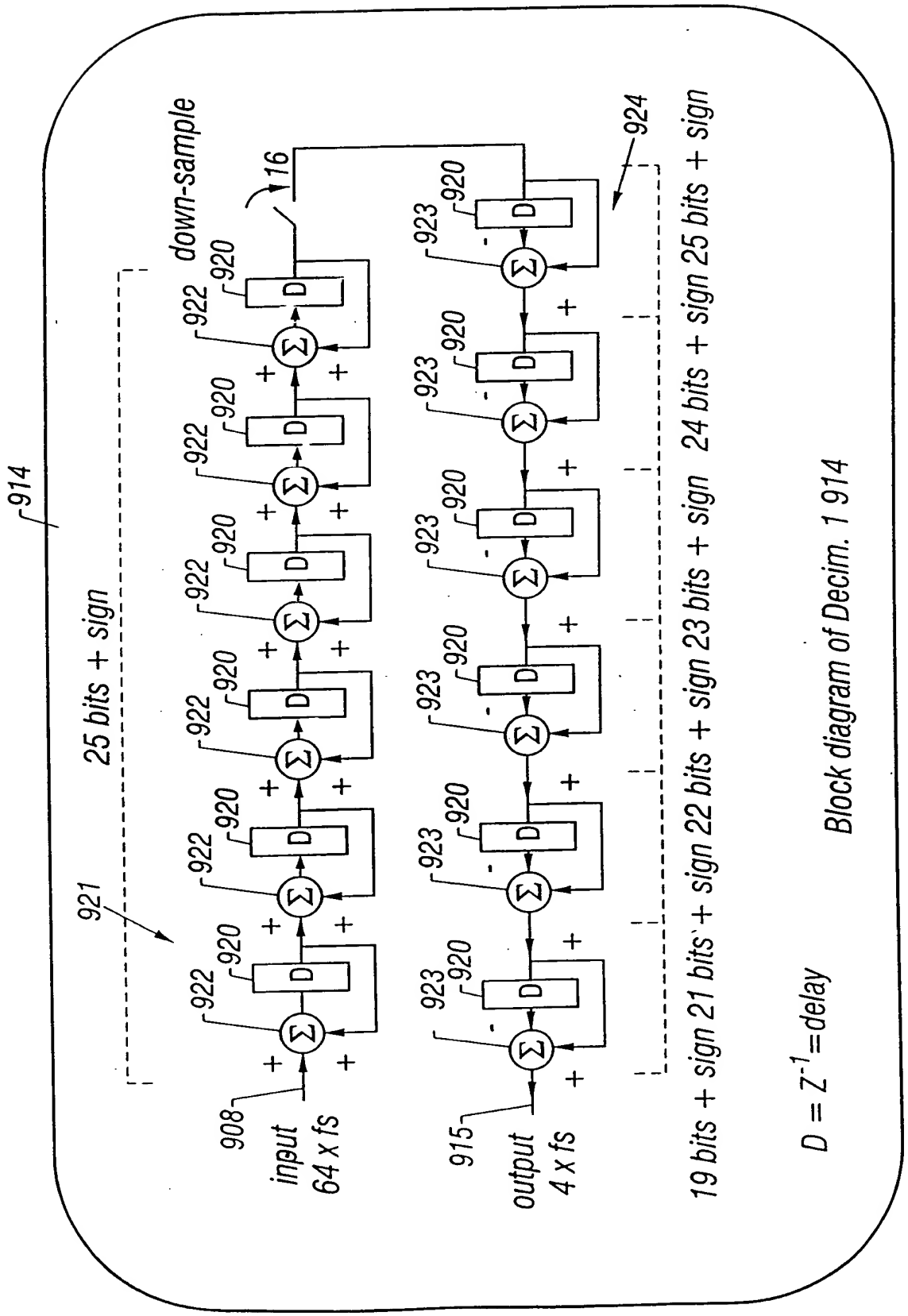

914
921
25 bits + sign
922
920
D
down-sample
16
924
923
908
input
64 x fs
915
output
4 x fs
19 bits + sign 21 bits + sign 22 bits + sign 23 bits + sign 24 bits + sign 25 bits + sign
D = Z-1=delay
Block diagram of Decim. 1 914

FIG. 89

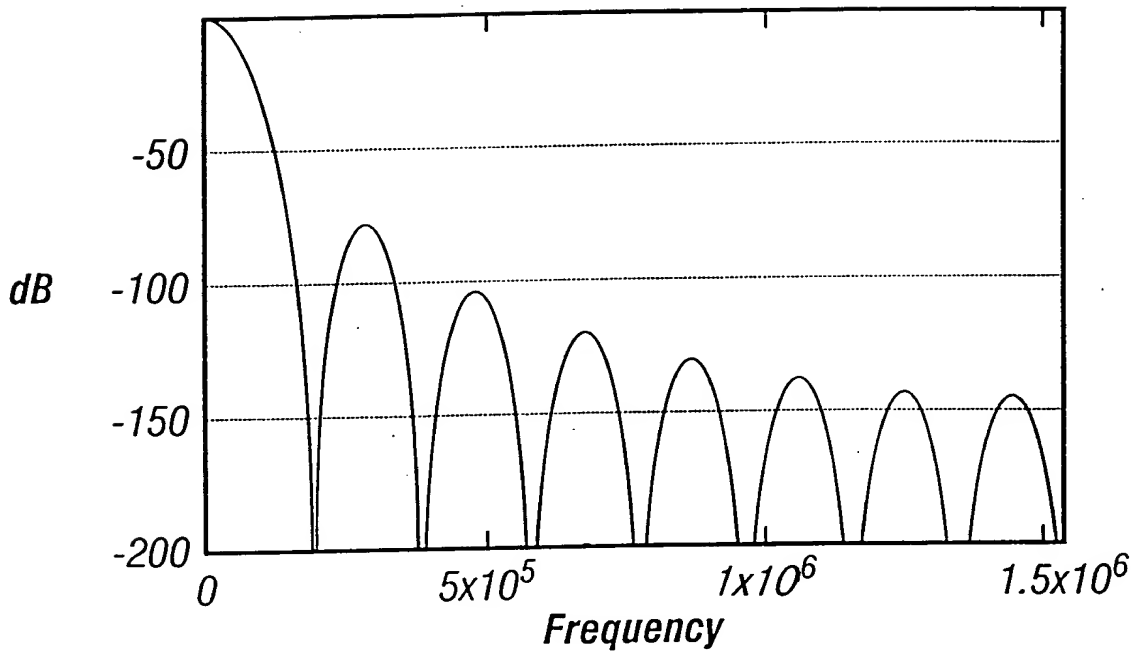

dB
-50
-100
-150
-200
0
5x10^5
1x10^6
1.5x10^6
Frequency

FIG. 90

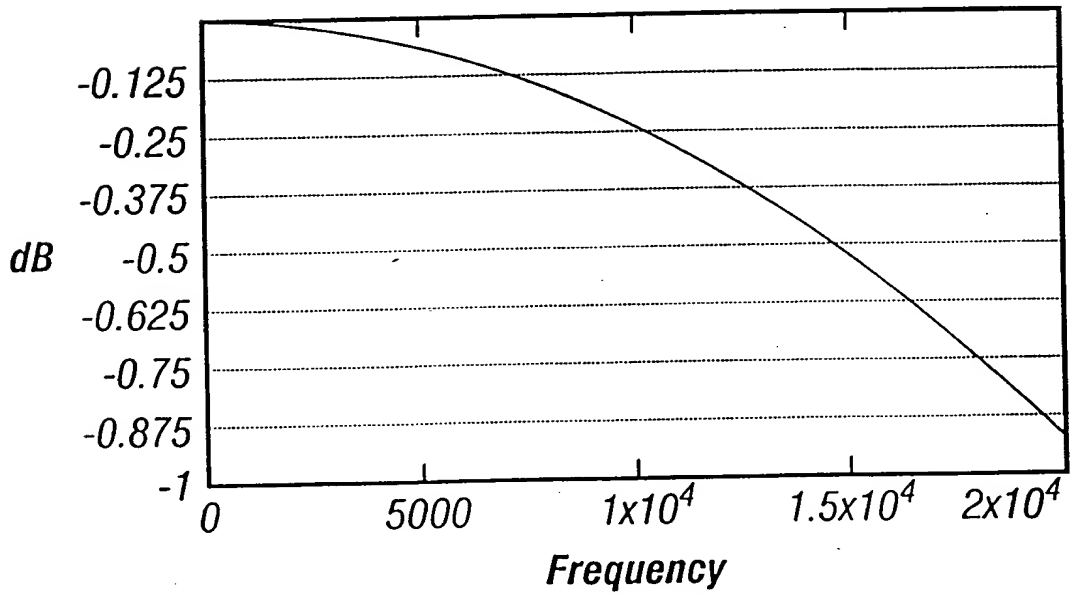

dB
-0.125
-0.25
-0.375
-0.5
-0.625
-0.75
-0.875
-1
0
5000
1x10^4
1.5x10^4
2x10^4
Frequency

FIG. 91

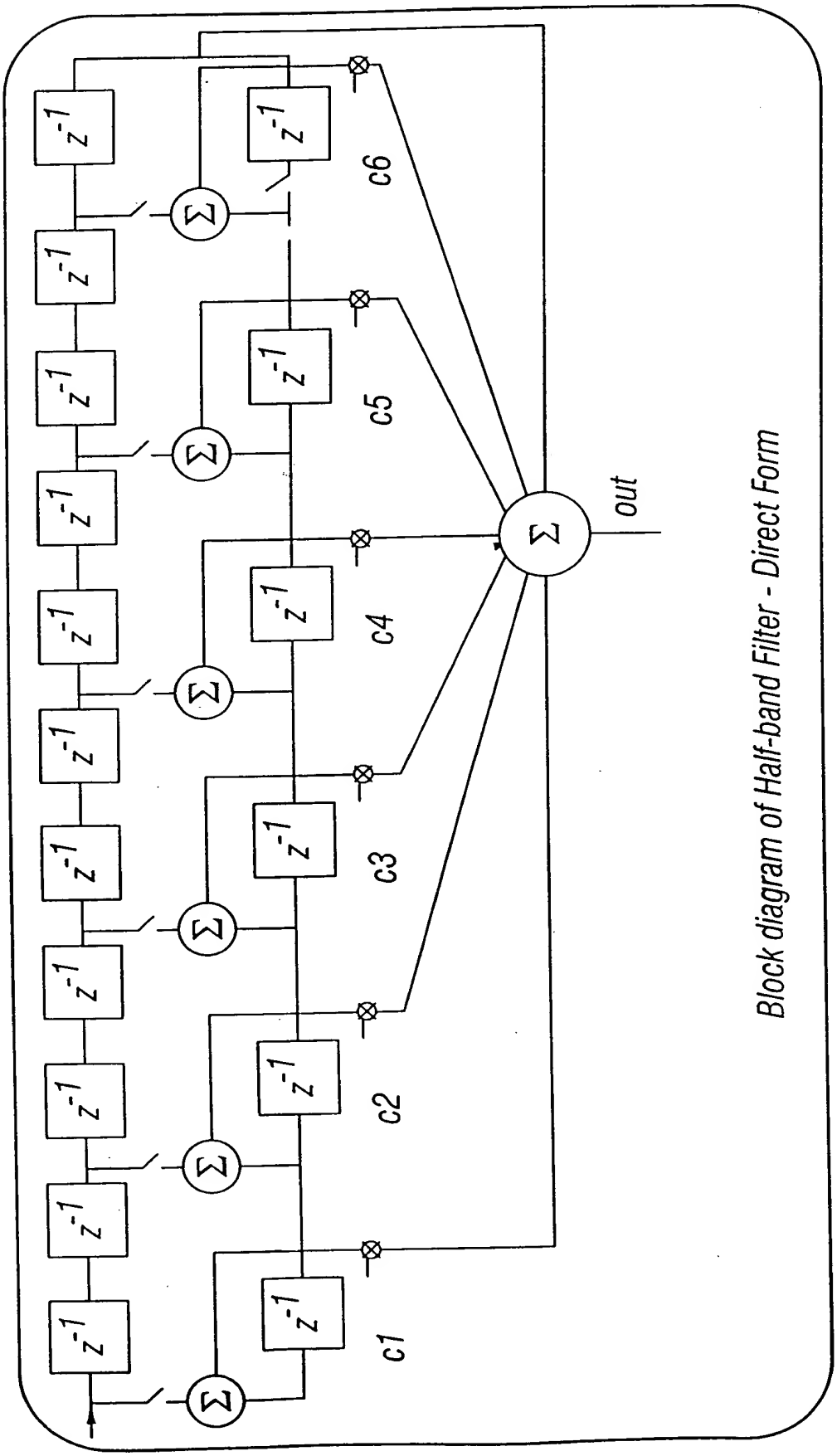

Block diagram of Half-band Filter - Direct Form
out
c1
c2
c3
c4
c5
c6
z-1
Σ

FIG. 92

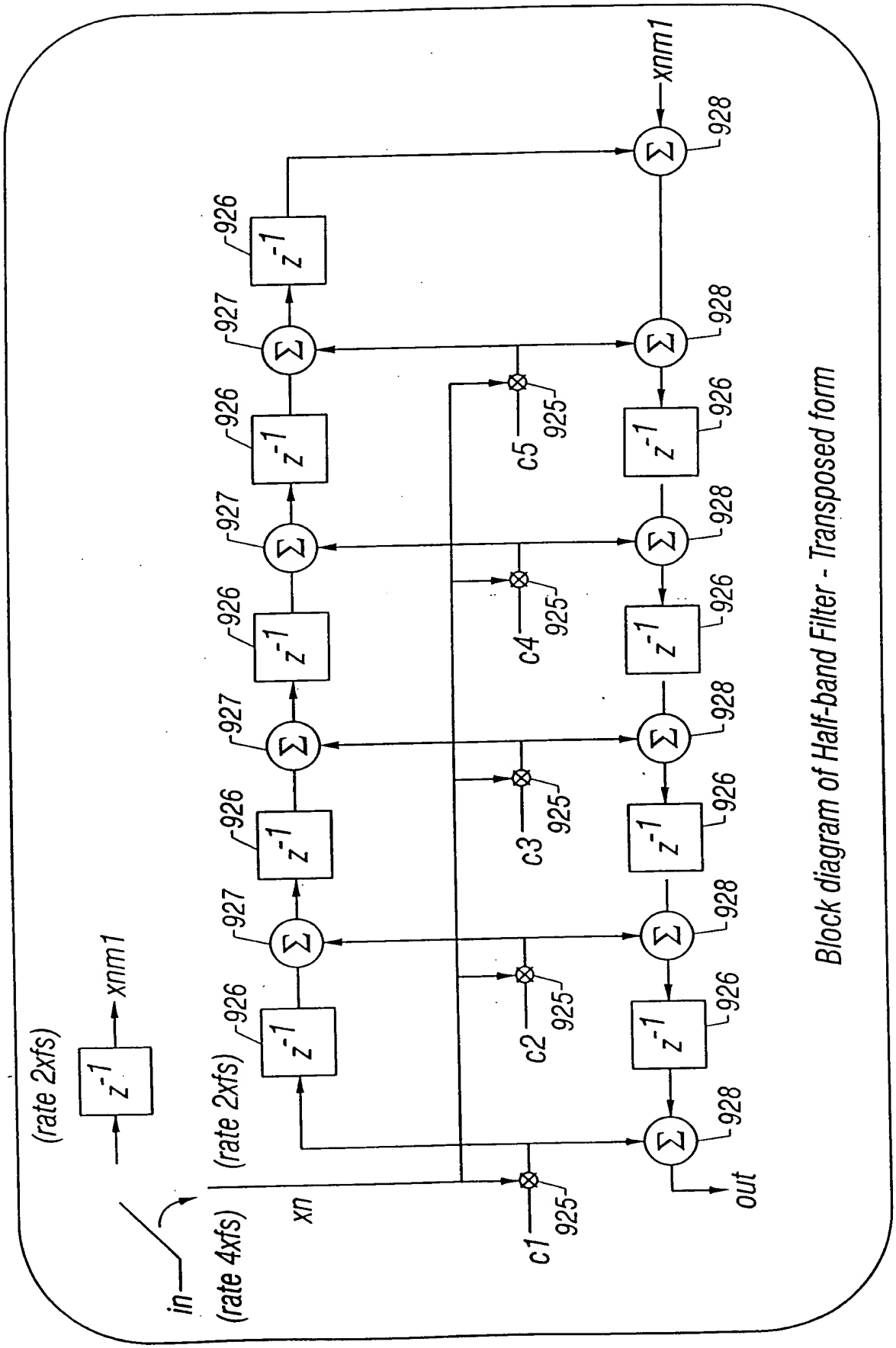

Block diagram of Half-band Filter - Transposed form
in
(rate 4xfs)
(rate 2xfs)
(rate 2xfs)
xn
xnm1
out
c1
c2
c3
c4
c5
925
926
927
928
z-1
Σ

FIG. 93

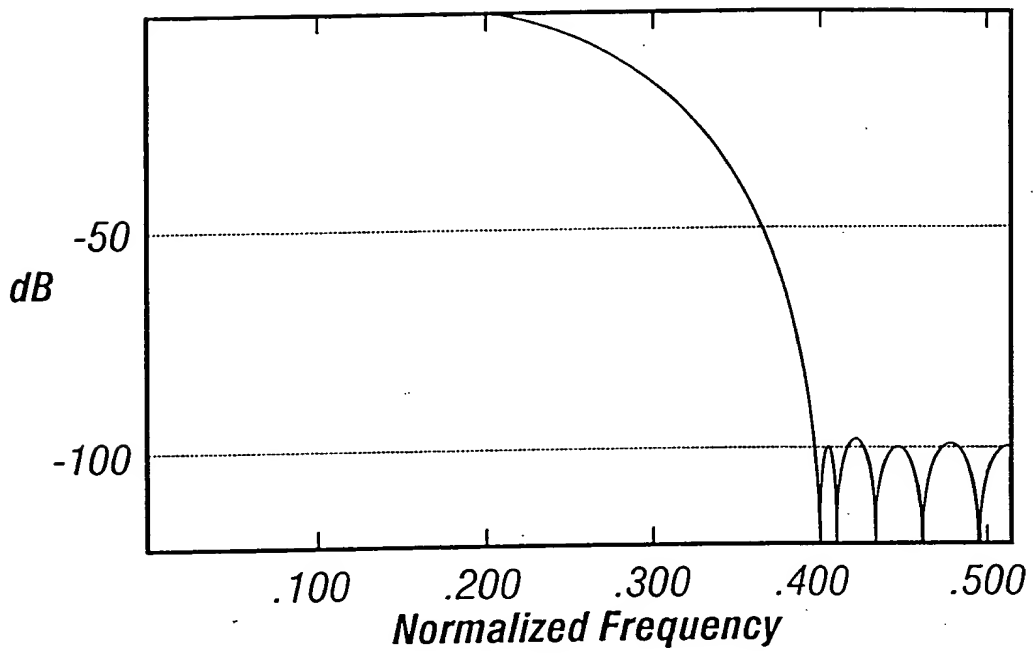

-50
dB
-100
.100
.200
.300
.400
.500
Normalized Frequency

FIG. 94

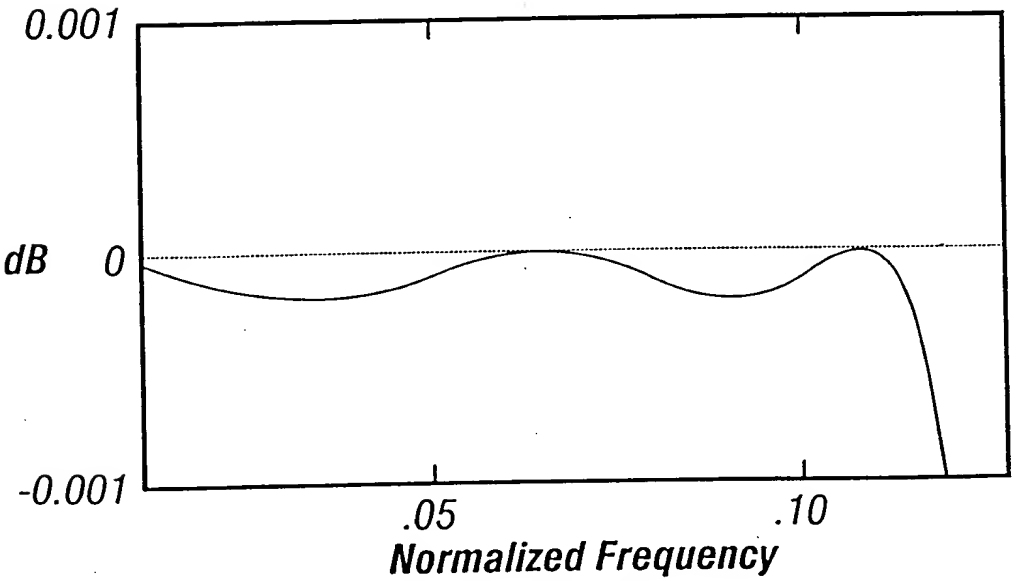

0.001
dB
0
-0.001
.05
.10
Normalized Frequency

FIG. 95

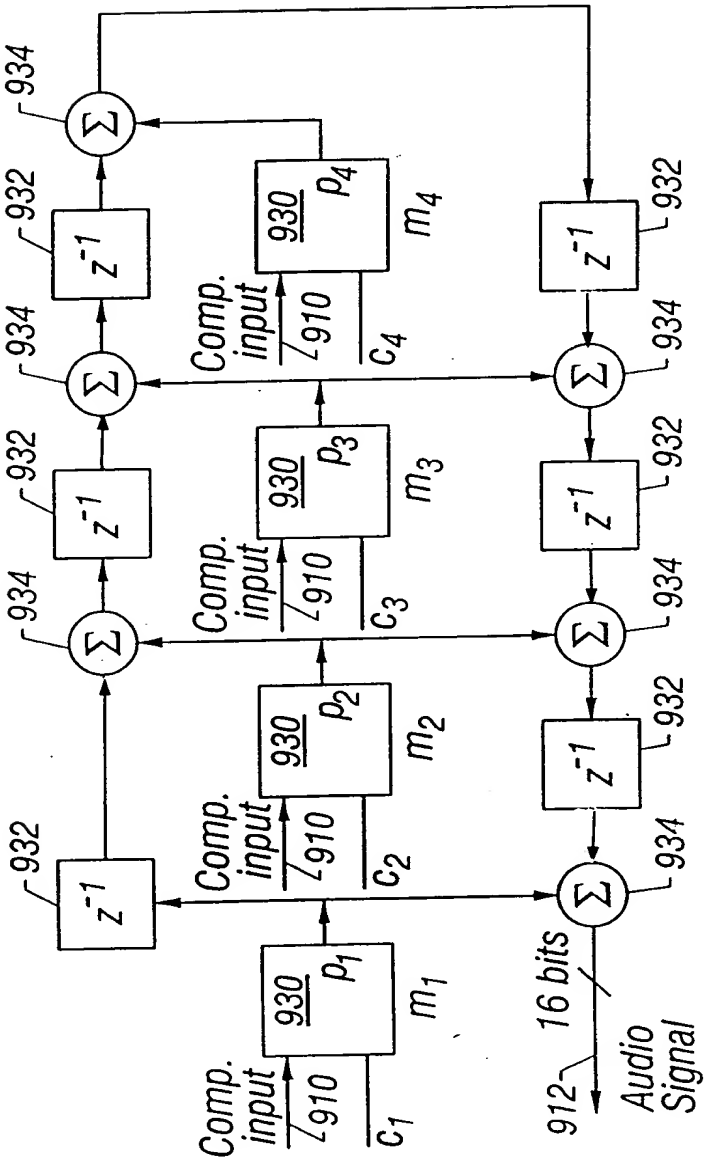

904
934
932
930
910
912
Comp. input
16 bits
Audio Signal
z^{-1}
p_1
p_2
p_3
p_4
m_1
m_2
m_3
m_4
c_1
c_2
c_3
c_4

FIG. 96

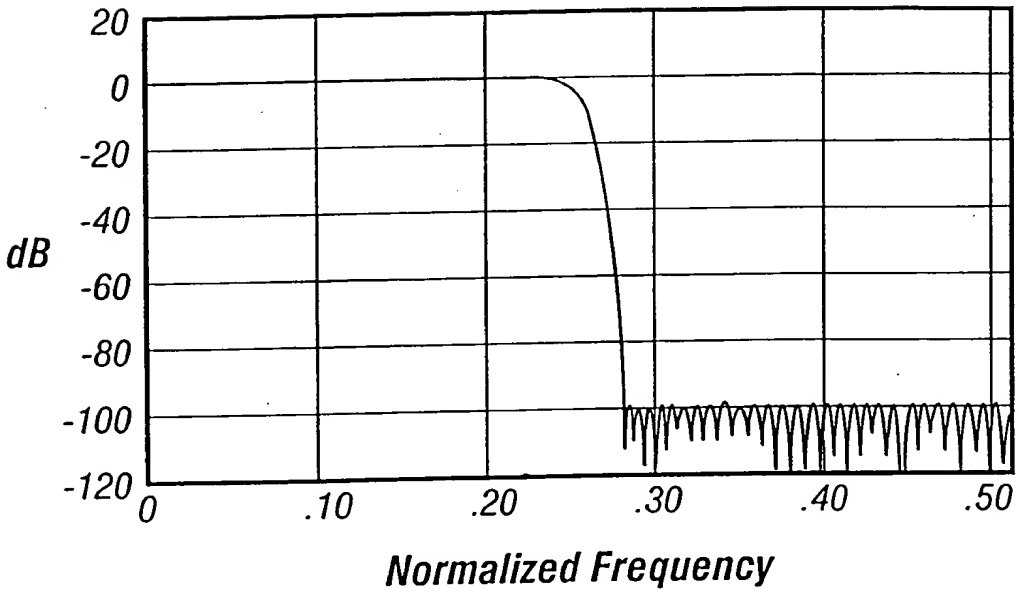

20
0
-20
-40
-60
-80
-100
-120
dB
0
.10
.20
.30
.40
.50
Normalized Frequency

FIG. 97

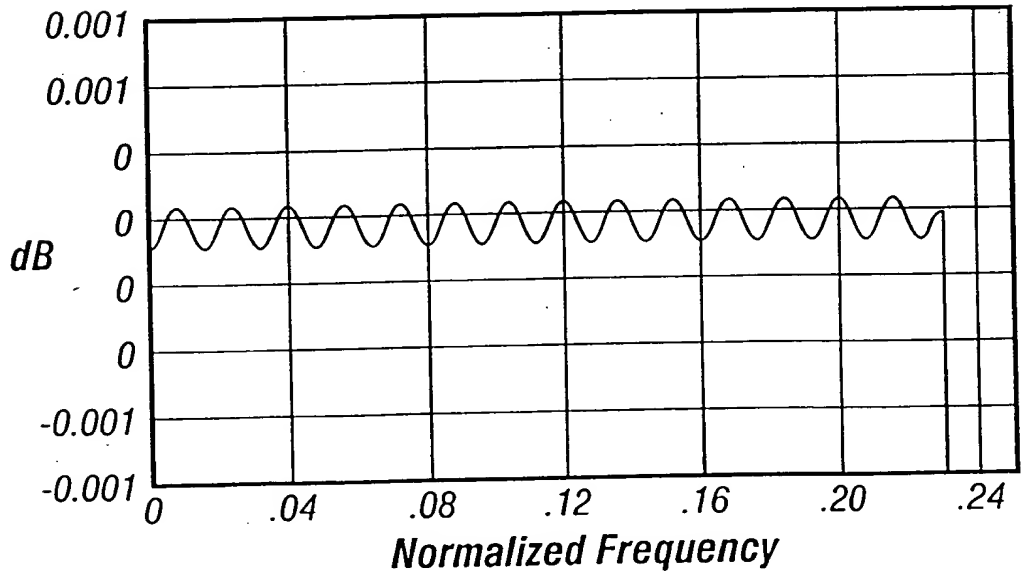

0.001
0.001
0
0
0
0
-0.001
-0.001
dB
0
.04
.08
.12
.16
.20
.24
Normalized Frequency

FIG. 98

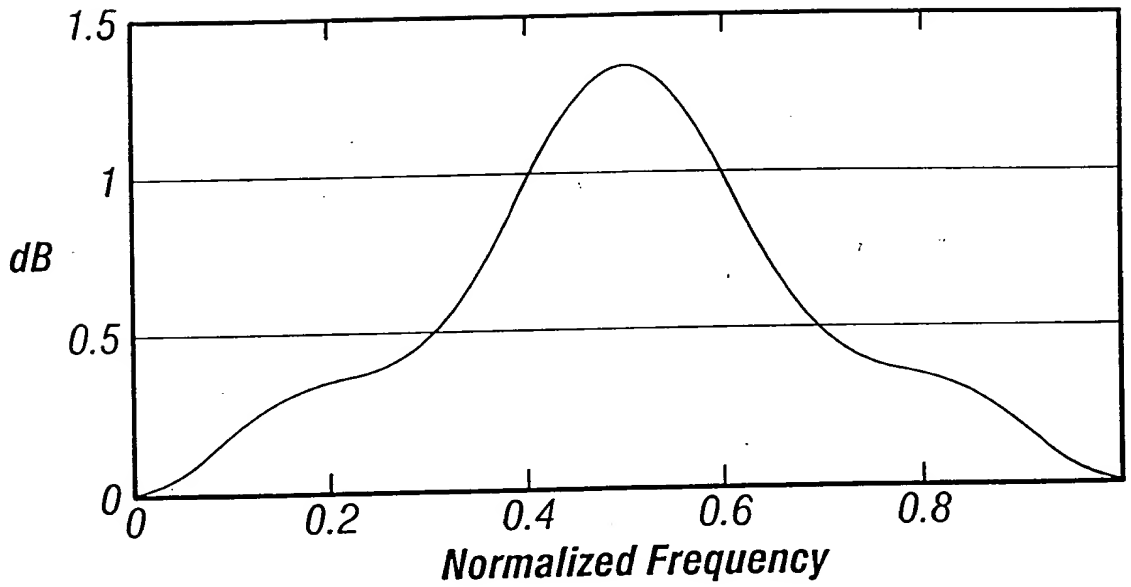


FIG. 99

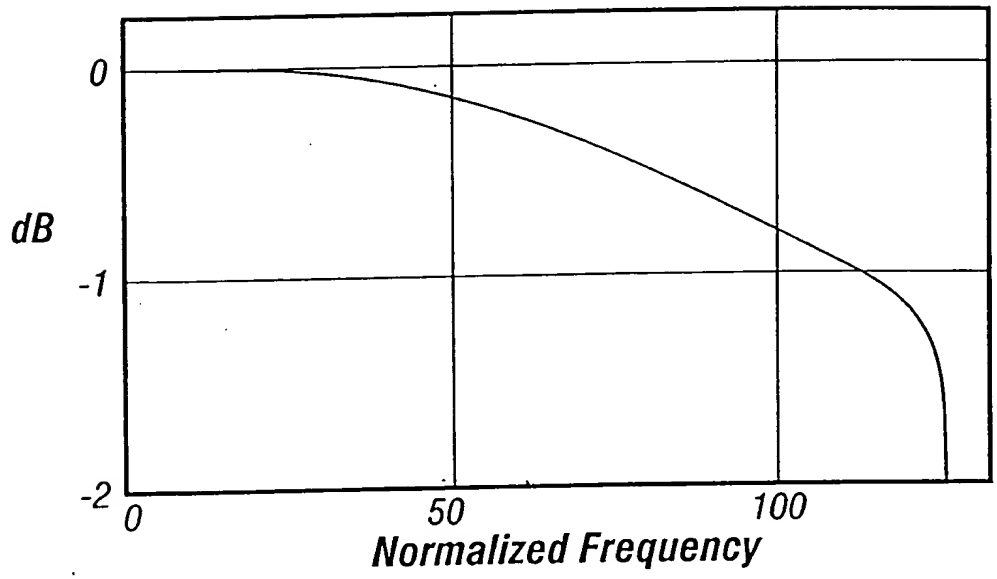


FIG. 100

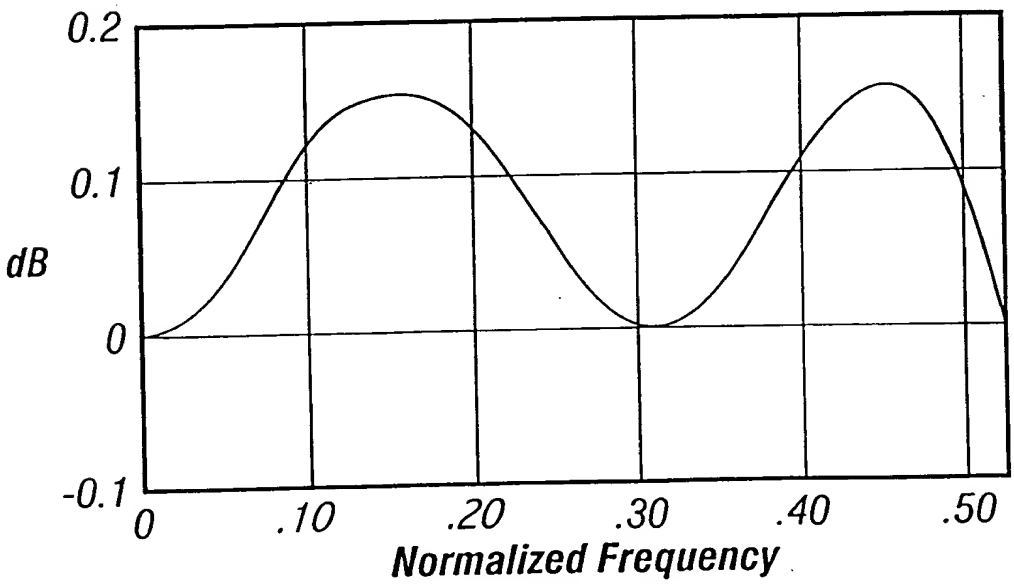


FIG. 101

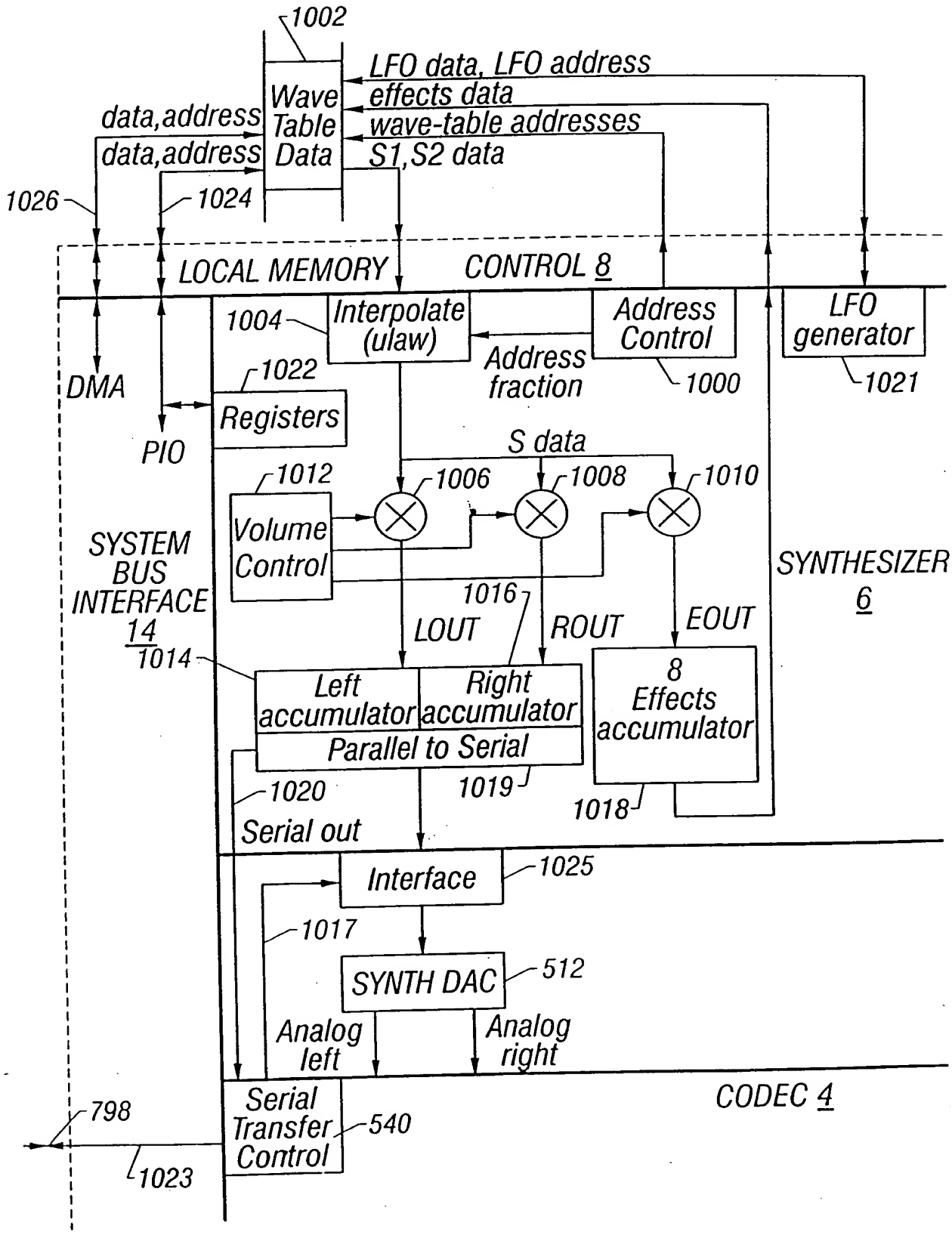

1002
Wave Table Data
LFO data, LFO address
effects data
wave-table addresses
S1,S2 data
data,address
data,address
1026
1024
LOCAL MEMORY
CONTROL 8
1004
Interpolate (ulaw)
Address Control
LFO generator
Address fraction
1000
1021
DMA
1022
Registers
PIO
S data
1012
1006
1008
1010
Volume Control
SYSTEM BUS INTERFACE 14
SYNTHESIZER 6
1016
LOUT
ROUT
EOUT
1014
Left accumulator
Right accumulator
8 Effects accumulator
Parallel to Serial
1020
1019
1018
Serial out
Interface
1025
1017
SYNTH DAC
512
Analog left
Analog right
CODEC 4
798
Serial Transfer Control
540
1023

FIG. 102

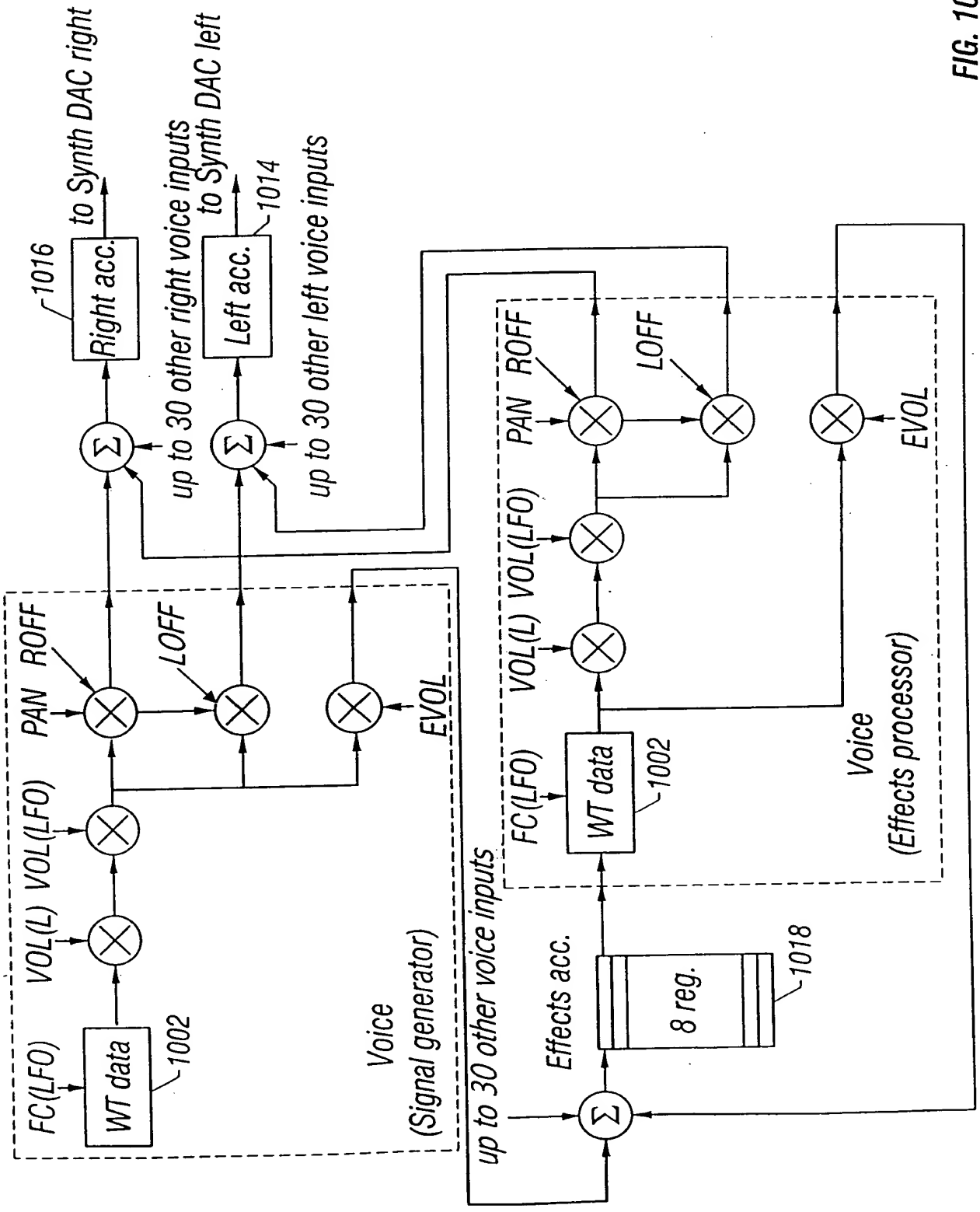

to Synth DAC right
to Synth DAC left
1016
Right acc.
1014
Left acc.
up to 30 other right voice inputs
up to 30 other left voice inputs
PAN
ROFF
LOFF
EVOL
FC(LFO)
VOL(L)
VOL(LFO)
WT data
1002
Voice
(Signal generator)
up to 30 other voice inputs
Effects acc.
8 reg.
1018
Voice
(Effects processor)

FIG. 103

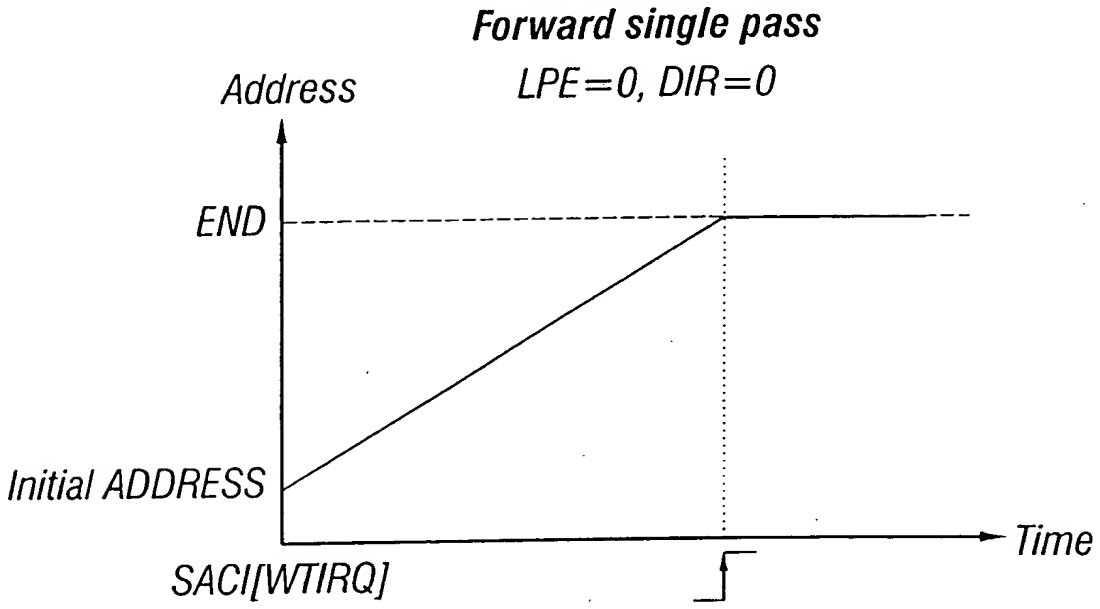


FIG. 104A

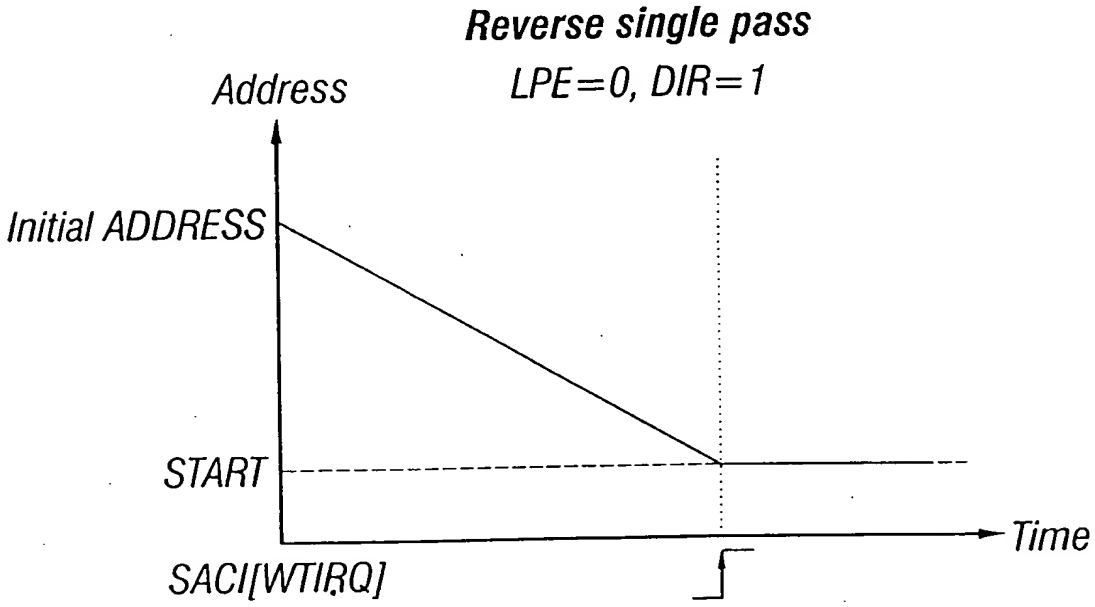


FIG. 104B

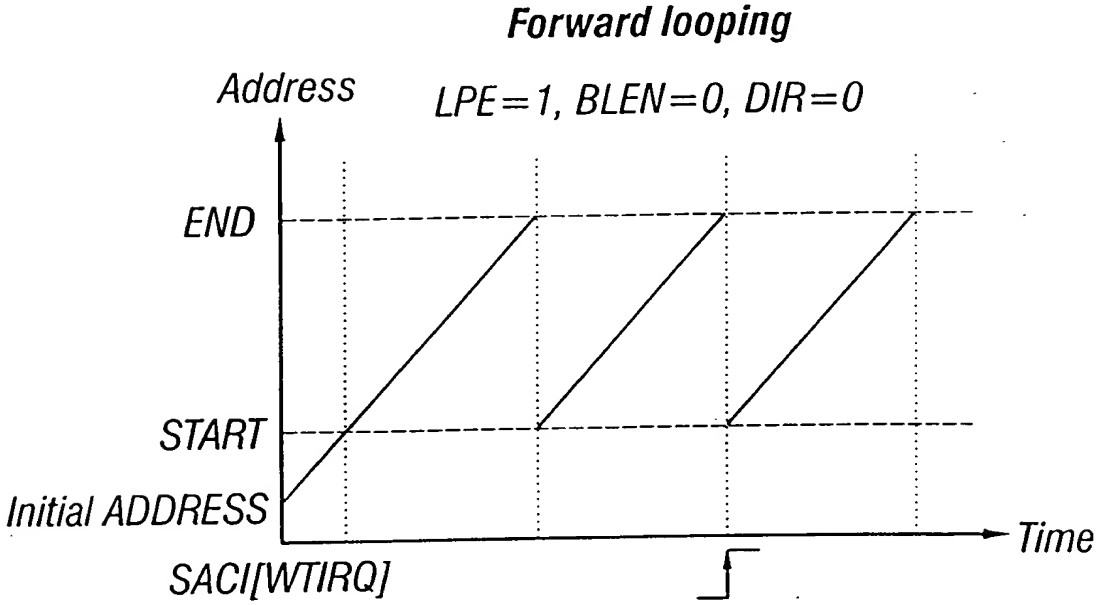


FIG. 104C

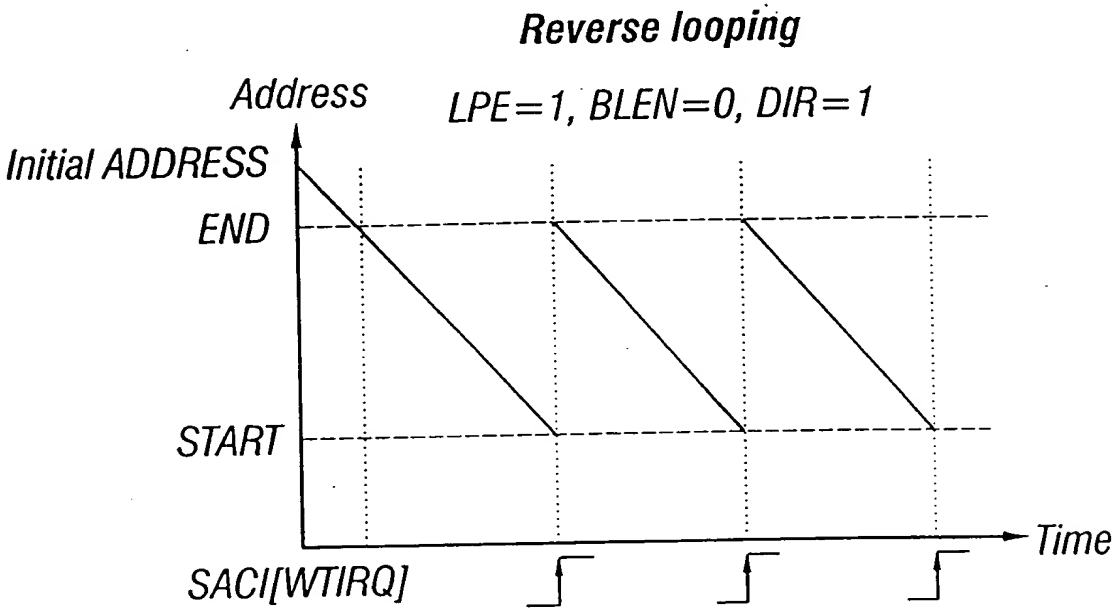


FIG. 104D

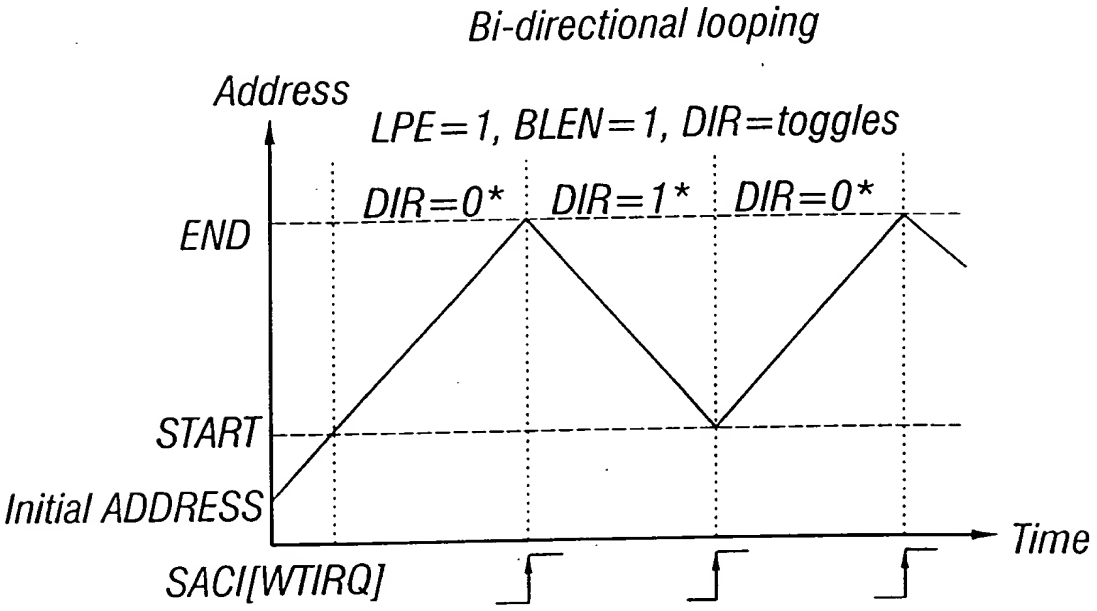


FIG. 104E

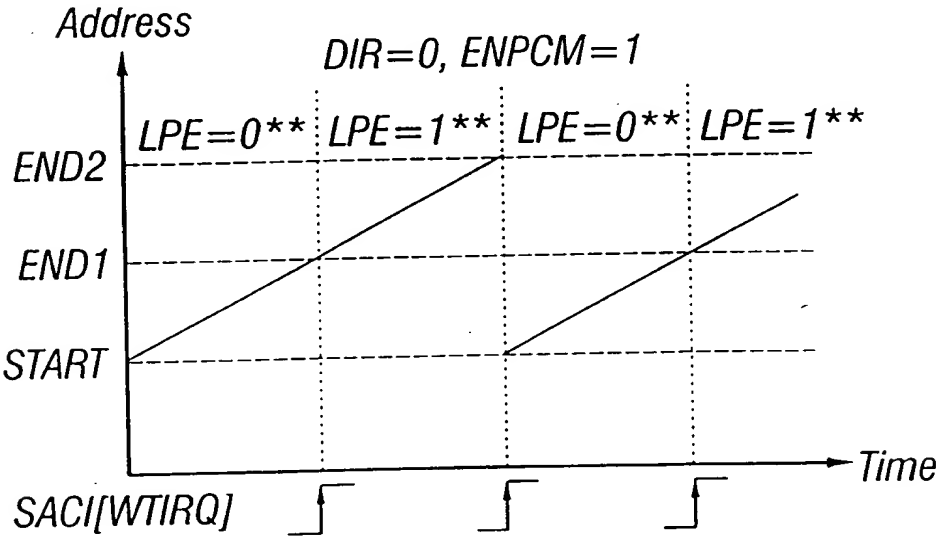


FIG. 104F

* indicates self-modifying
** indicates program modification

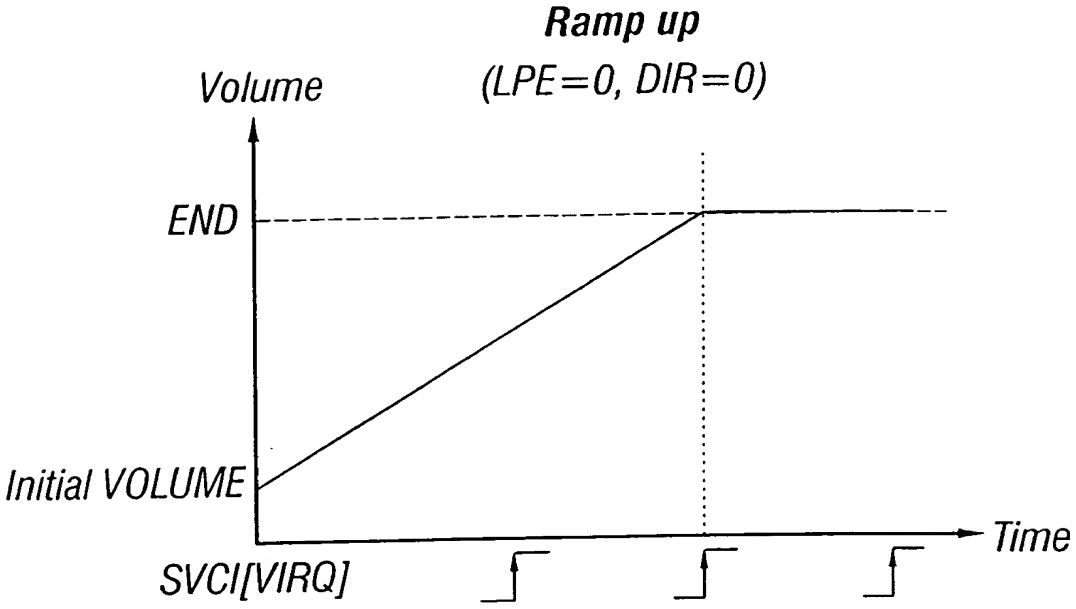


FIG. 105A

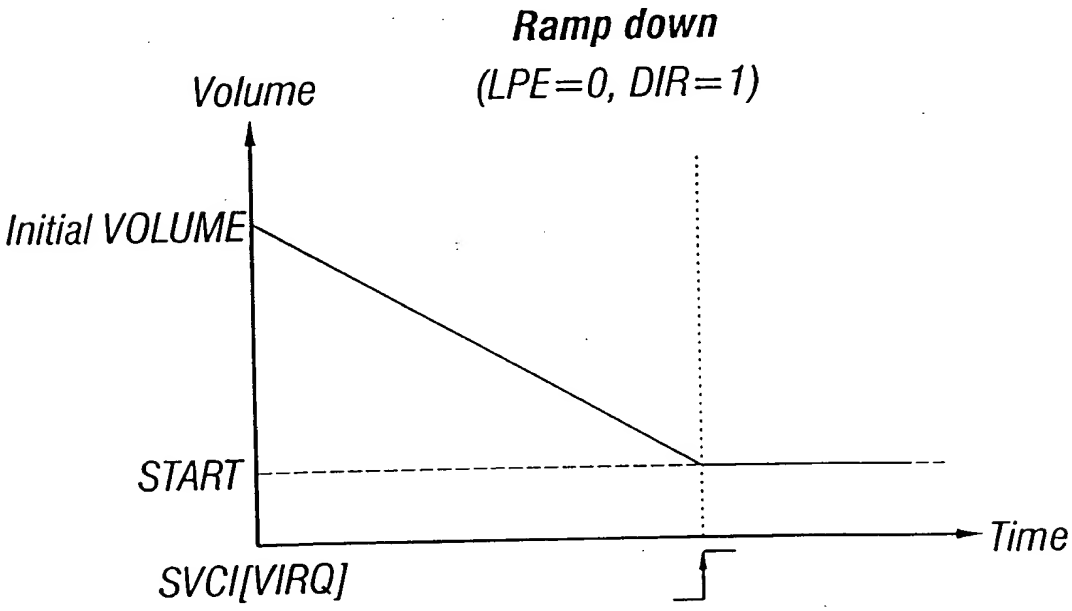


FIG. 105B

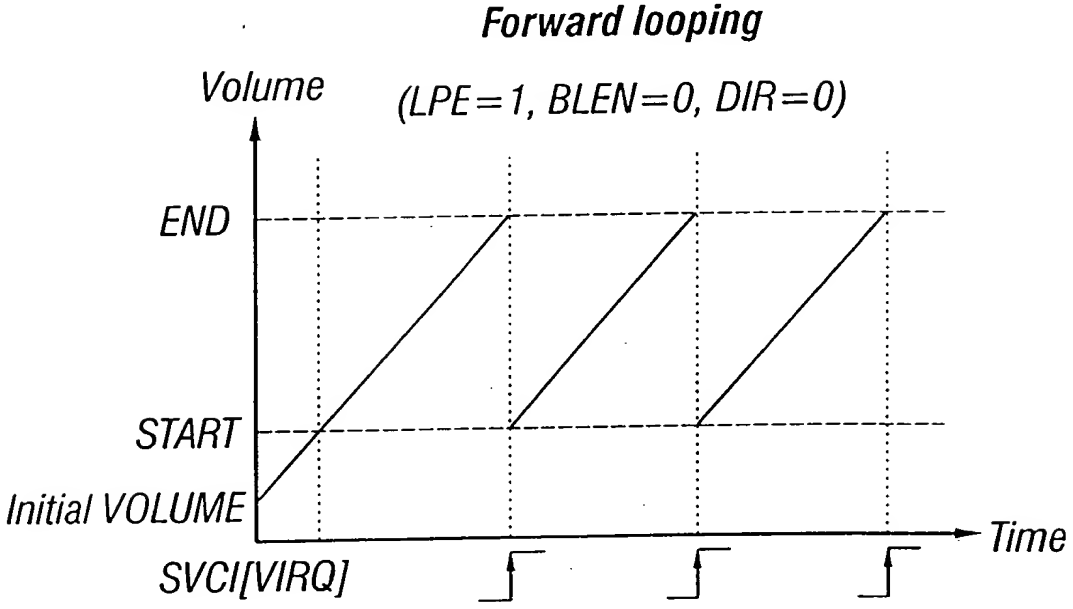


FIG. 105C

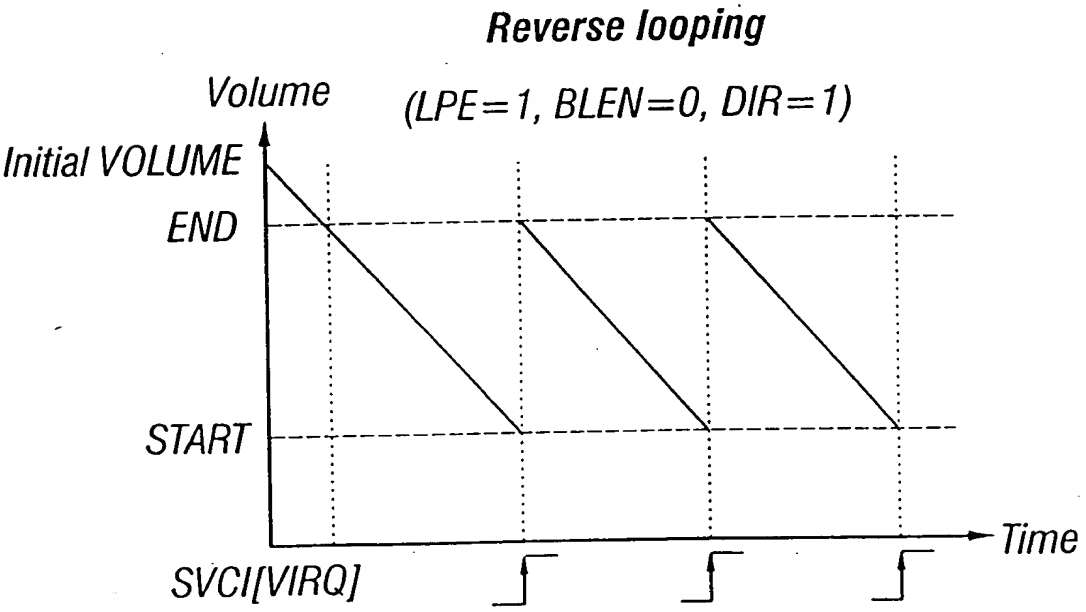


FIG. 105D

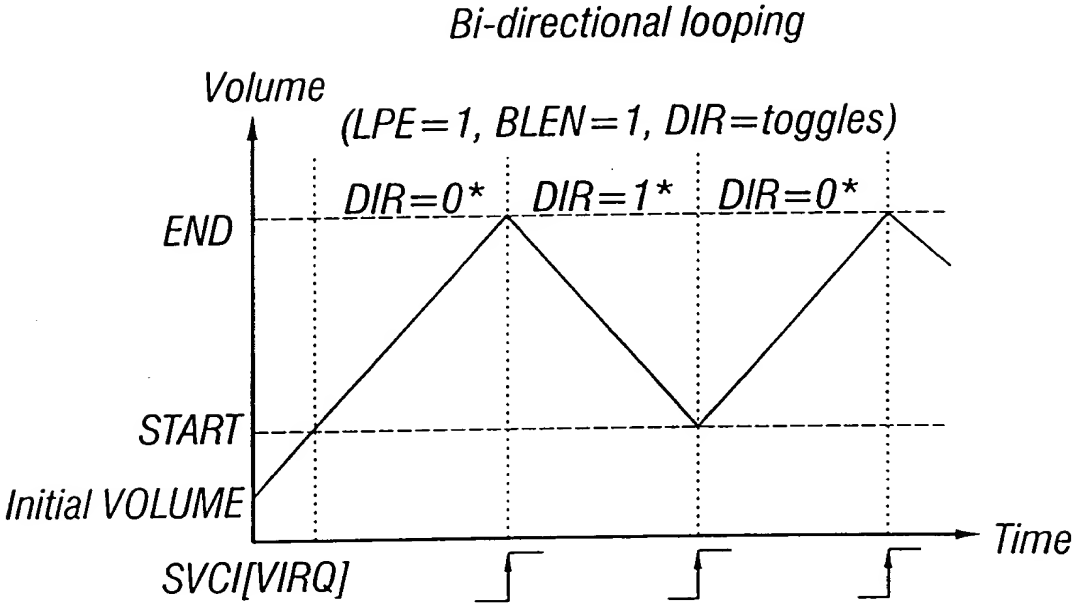


FIG. 105E

* indicates self-modifying

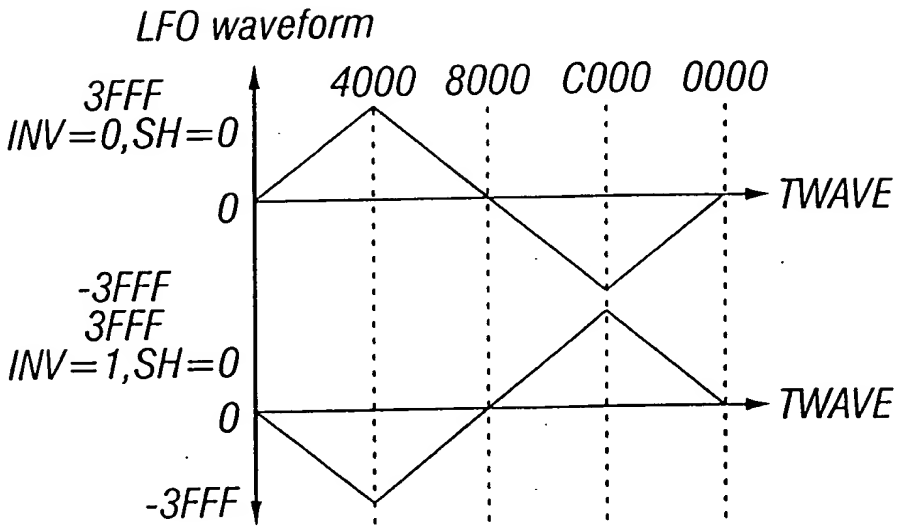


FIG. 106A

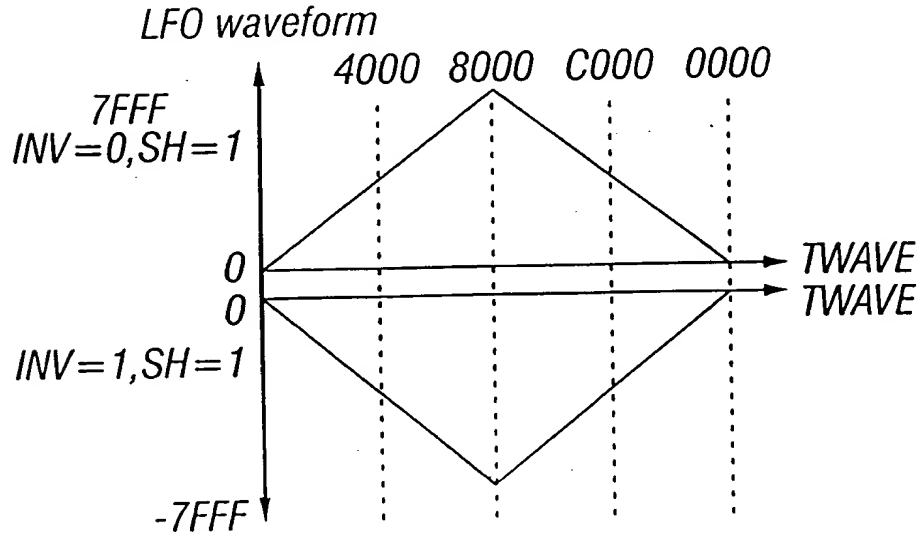


FIG. 106B

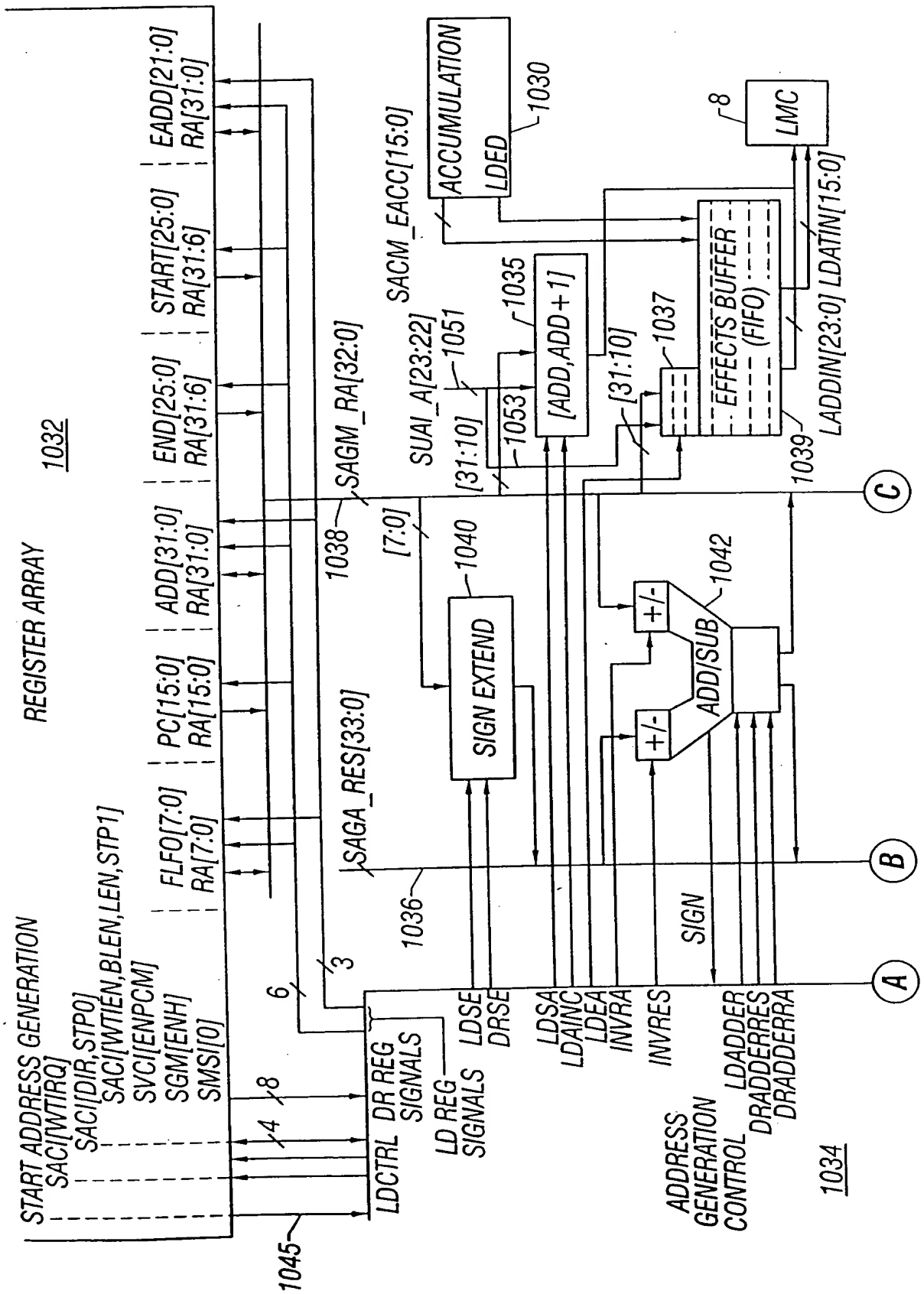

START ADDRESS GENERATION
SAC[WTIRQ]
SAC[DIR,STP0]
SAC[WTIEN,BLEN,LEN,STP1]
SVC[ENPCM]
SGM[ENH]
SMS[0]
1045
REGISTER ARRAY
1032
FLFO[7:0]
RA[7:0]
PC[15:0]
RA[15:0]
ADD[31:0]
RA[31:0]
END[25:0]
RA[31:6]
START[25:0]
RA[31:6]
EADD[21:0]
RA[31:0]
8
4
6
3
LDCTRL
DR REG SIGNALS
LD REG SIGNALS
LDSE
DRSE
LDSA
LDAINC
LDEA
INVRA
INVRES
SIGN
ADDRESS GENERATION CONTROL
LDADDER
DRADDERRES
DRADDERRA
1034
1036
SAGA_RES[33:0]
1038
SAGM_RA[32:0]
[7:0]
1040
SIGN EXTEND
SUAI_A[23:22]
1051
[31:10]
1053
SACM_EACC[15:0]
ACCUMULATION
LDED
1030
[ADD,ADD+1]
1035
[31:10]
1037
+/-
+/-
ADD/SUB
1042
EFFECTS BUFFER
(FIFO)
1039
8
LMC
LADDIN[23:0]
LDATIN[15:0]
A
B
C

FIG. 107A

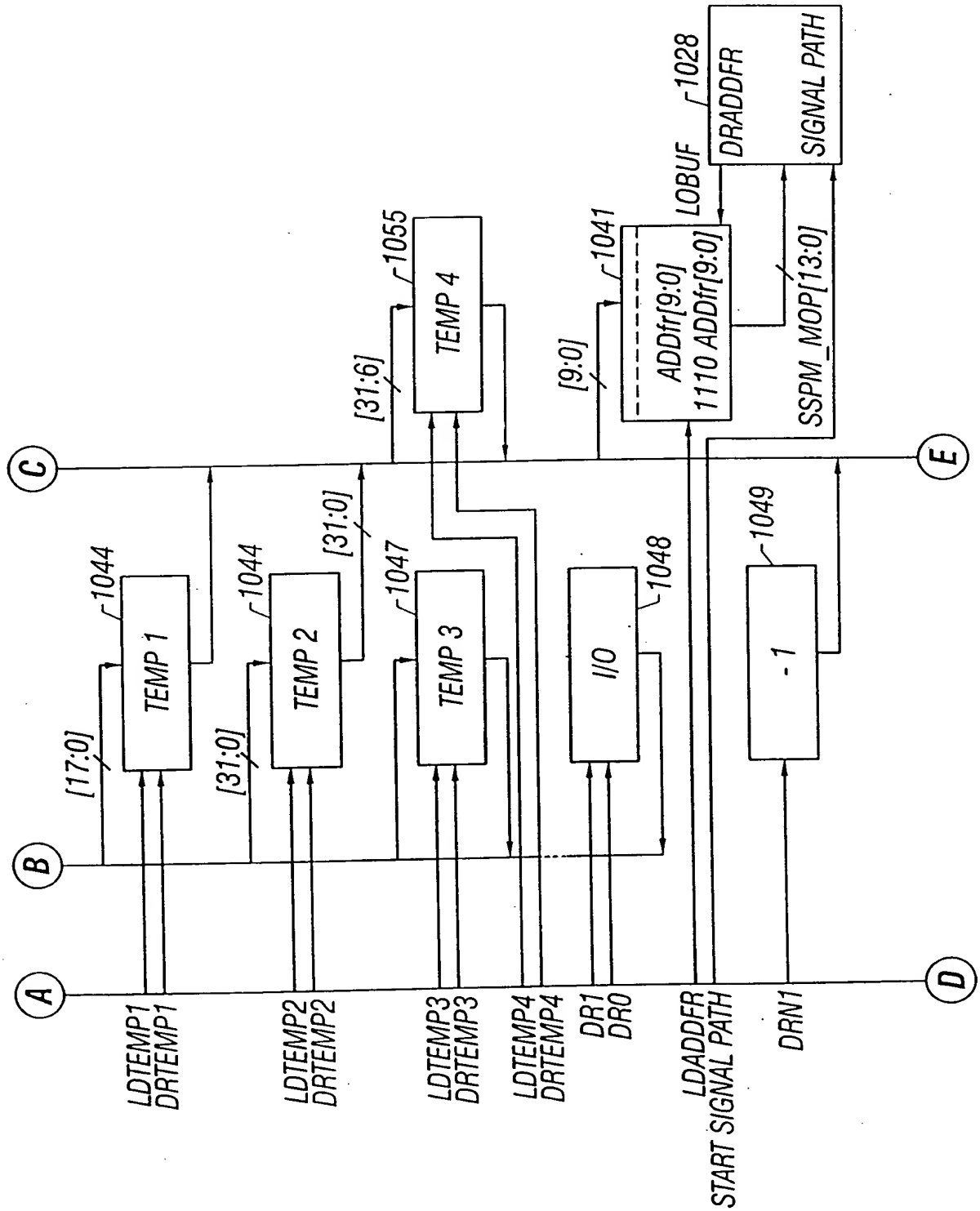

A
B
C
D
E
[17:0]
1044
TEMP 1
[31:0]
1044
TEMP 2
[31:0]
1047
TEMP 3
[31:6]
1055
TEMP 4
I/O
1048
[9:0]
1041
ADDfr[9:0]
1110 ADDfr[9:0]
LOBUF
1028
DRADDFR
SIGNAL PATH
SSPM_MOP[13:0]
1049
-1
LDTEMP1
DRTEMP1
LDTEMP2
DRTEMP2
LDTEMP3
DRTEMP3
LDTEMP4
DRTEMP4
DR1
DR0
LDADDFR
START SIGNAL PATH
DRN1

FIG. 107B

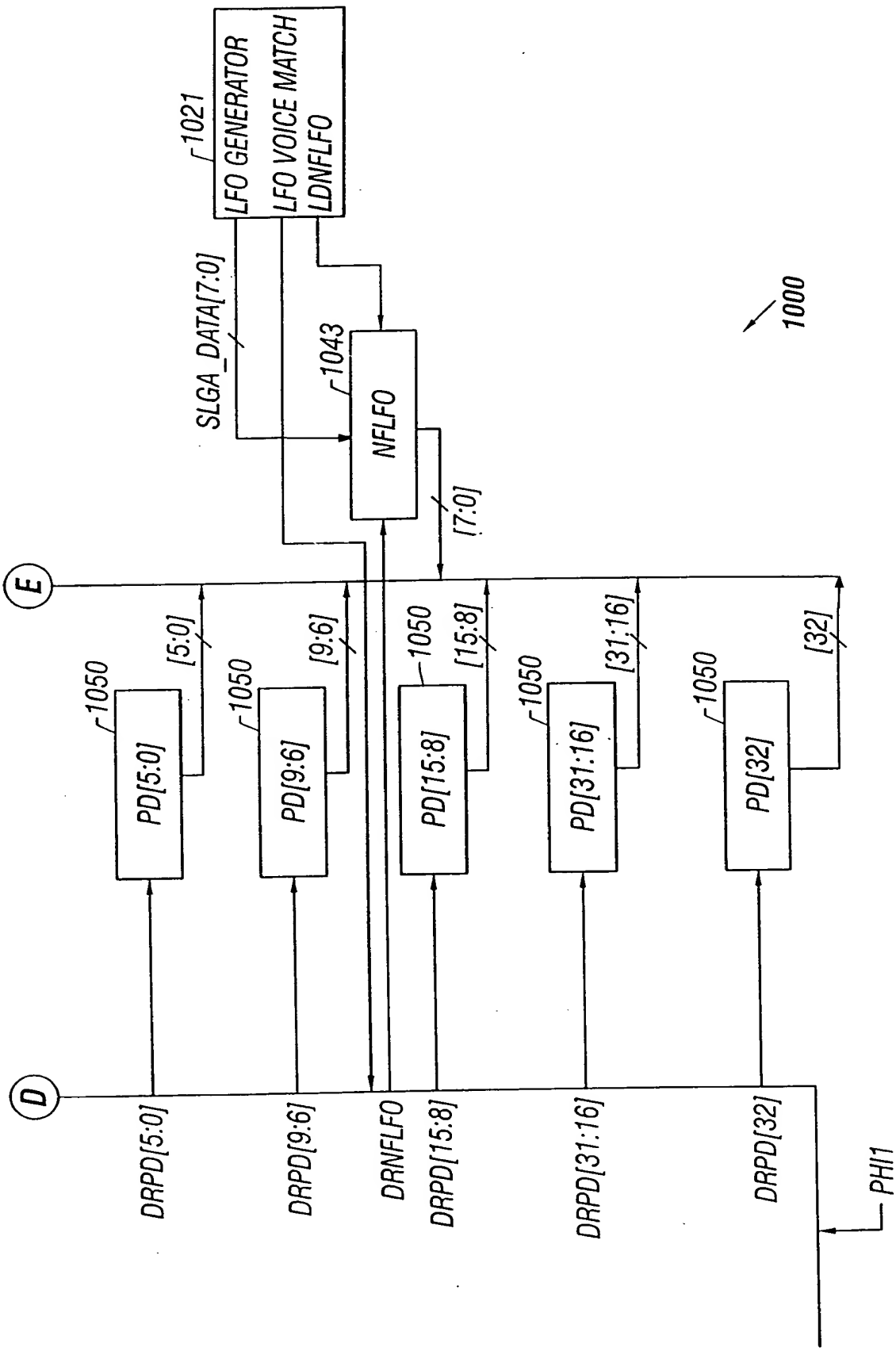

1021
LFO GENERATOR
LFO VOICE MATCH
LDNFLFO
SLGA_DATA[7:0]
1043
NFLFO
[7:0]
1000
E
D
1050
PD[5:0]
[5:0]
1050
PD[9:6]
[9:6]
1050
PD[15:8]
[15:8]
1050
PD[31:16]
[31:16]
1050
PD[32]
[32]
DRPD[5:0]
DRPD[9:6]
DRNFLFO
DRPD[15:8]
DRPD[31:16]
DRPD[32]
PHI1

FIG. 107C

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

For normal modes

Clock #	Result bus	op	Reg. array bus	equation	comments
1			FLFO		• load register array with next value from LFO generator if LFO and voice match
2	sign extended FLFO	+ 18s	FC	FC(LFO)= FC+FLFO	
3	[+,-] result	+ 34s	ADD	NADD= ADD±FC(LFO)	• invert result based on DIR • load ADD into register to drive LMC • load ADDfr into register to drive Signal Path
4	[+,-] (result => temp2)	+ 34s	[+END, -START]	[-NADD+END, NADD-START]	• choose [+END, -START] based on LPE, BLEN, DIR • latch sign of operation • sign=1 indicates NADD>END or NADD<START
5	result				
6	result				

FIG. 108A-1

For normal modes

Clock #	Result bus	op	Reg. array bus	equation	comments
7	[+,-] result	+ 34s	[START, END]	[START, END] ±[±NADD ±[START, END]	• choose [+,-] and [END, START] based on LPE, BLEN and DIR • load ADD+1 into register to drive LMC
8	result		[result, temp2]		• choose [result, temp2] based on latched sign values above • upper bits truncate to get 32 bit unsigned result
9					
10					
11					
12					

FIG. 108A-2

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

For Boundary mirror mode (ENH=1, ENPCM=1,LPE=1)

Clock #	Result bus	op	Reg. array bus	equation	comments
1			FLFO		• load register array with next value from LFO generator if LFO and voice match
2	sign extended FLFO	+ 18s	FC	FC(LFO)= FC+FLFO	
3	(result=> temp1)	+ 34s	ADD	NADD= ADD±FC(LFO)	• load ADD into register to drive LMC • load ADDfr into register to drive Signal Path
4	(result=> temp2)	+ 34s	-END	NADD-END	
5	(result=> temp3)	+ 34s	-temp1	ADD-END	• latch sign of operation • sign=0 indicates ADD≥END
6	temp3	+ 34s	-1	NADD-END-1	• latch sign of operation •sign=0 indicates NADD≥END+1

FIG. 108B-1

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

For Boundary mirror mode (ENH=1, ENPCM=1, LPE=1)

Clock #	Result bus	op	Reg. array bus	equation	comments
7	result	+ 34s	START=> temp4	START + (NADD-END-1)	• load ADD+1 into register if sign=1 in operation 5 or START if sign=0, register will drive LMC • load START into temp4 for operation 12
8	result		[result, temp2]		• choose [result, temp2] based on latched sign value of operation 6 above • upper bits truncate to get 32 bit unsigned result
9	0	+ 33s	EADD		• load EADD into Effects buffer based on SMSI[0]

FIG. 108B-2

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

For Boundary mirror mode (ENH=1, ENPCM=1, LPE=1)

Clock #	Result bus	op	Reg. array bus	equation	comments
10	result=EADD, EADD=> temp2	+ 33s	-END	EADD-END	• latch sign of operation • sign=0 indicates if EADD ≥ END • load EADD into temp2 for operation 11
11	1	+ 34s	temp2=EADD	NEADD +EADD+1	
12			[temp4=START, result]		• choose [START, result] based on latched sign above • upper bits truncate to get 32 bit unsigned result

FIG. 108B-3

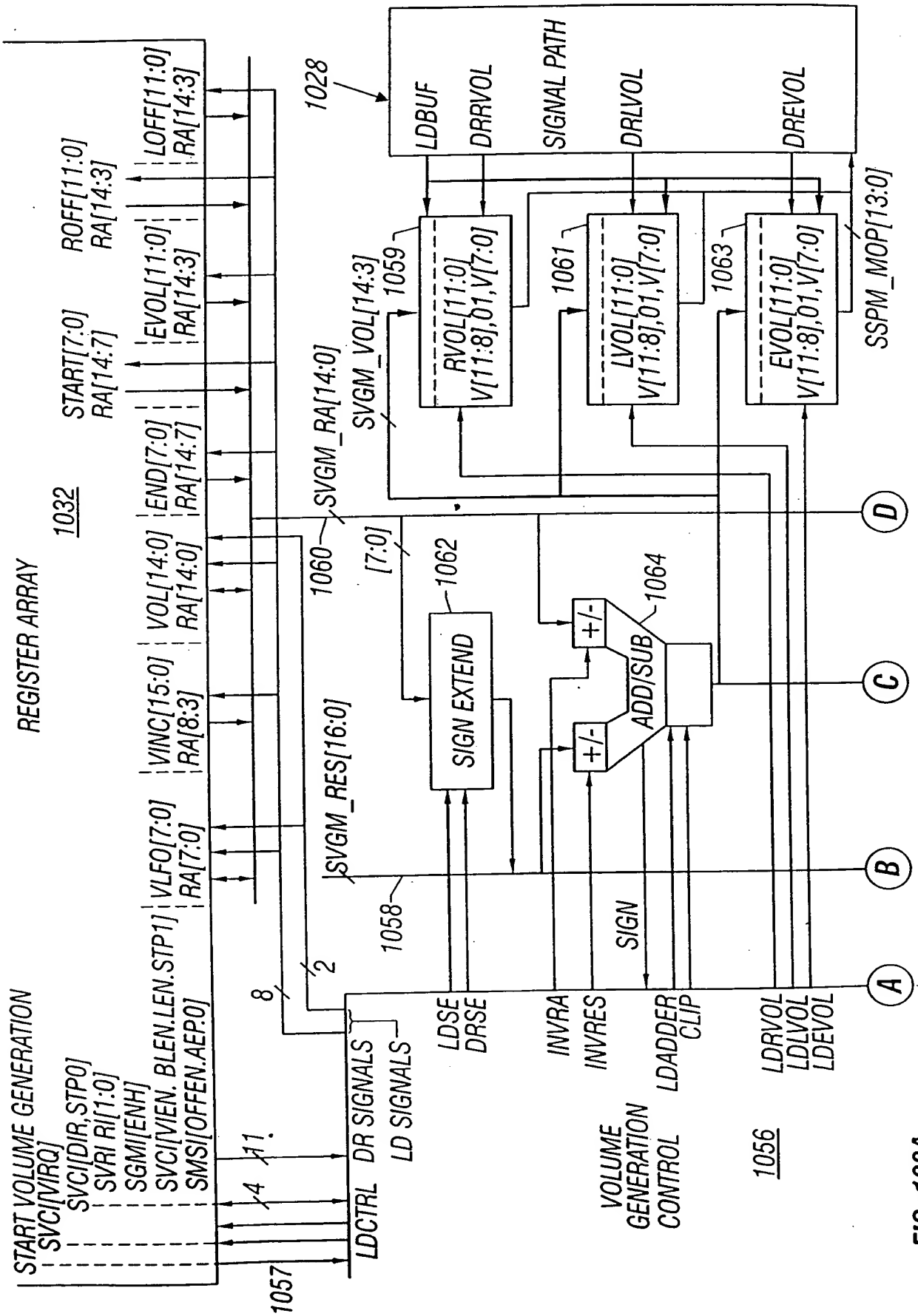

START VOLUME GENERATION
SVC[VIRQ]
SVC[DIR,STPO]
SVRI RI[1:0]
SGMI[ENH]
SVC[VIEN, BLEN,LEN,STP1]
SMS[OFFEN,AEP0]
VLFO[7:0] RA[7:0]
VINC[15:0] RA[8:3]
VOL[14:0] RA[14:0]
END[7:0] RA[14:7]
START[7:0] RA[14:7]
EVOL[11:0] RA[14:3]
ROFF[11:0] RA[14:3]
LOFF[11:0] RA[14:3]
REGISTER ARRAY
1032
1057
LDCTRL
DR SIGNALS
LD SIGNALS
1058
SVGM_RES[16:0]
1060
SVGM_RA[14:0]
[7:0]
SVGM_VOL[14:3]
1059
1061
1063
1028
LDBUF
DRRVOL
SIGNAL PATH
DRLVOL
DREVOL
SSPM_MOP[13:0]
RVOL[11:0] V[11:8],01,V[7:0]
LVOL[11:0] V[11:8],01,V[7:0]
EVOL[11:0] V[11:8],01,V[7:0]
1062
SIGN EXTEND
1064
+/-
+/-
ADD/SUB
A
B
C
D
LDSE
DRSE
INVRA
INVRES
SIGN
LDADDER
CLIP
LDRVOL
LDLVOL
LDEVOL
VOLUME GENERATION CONTROL
1056

FIG. 109A

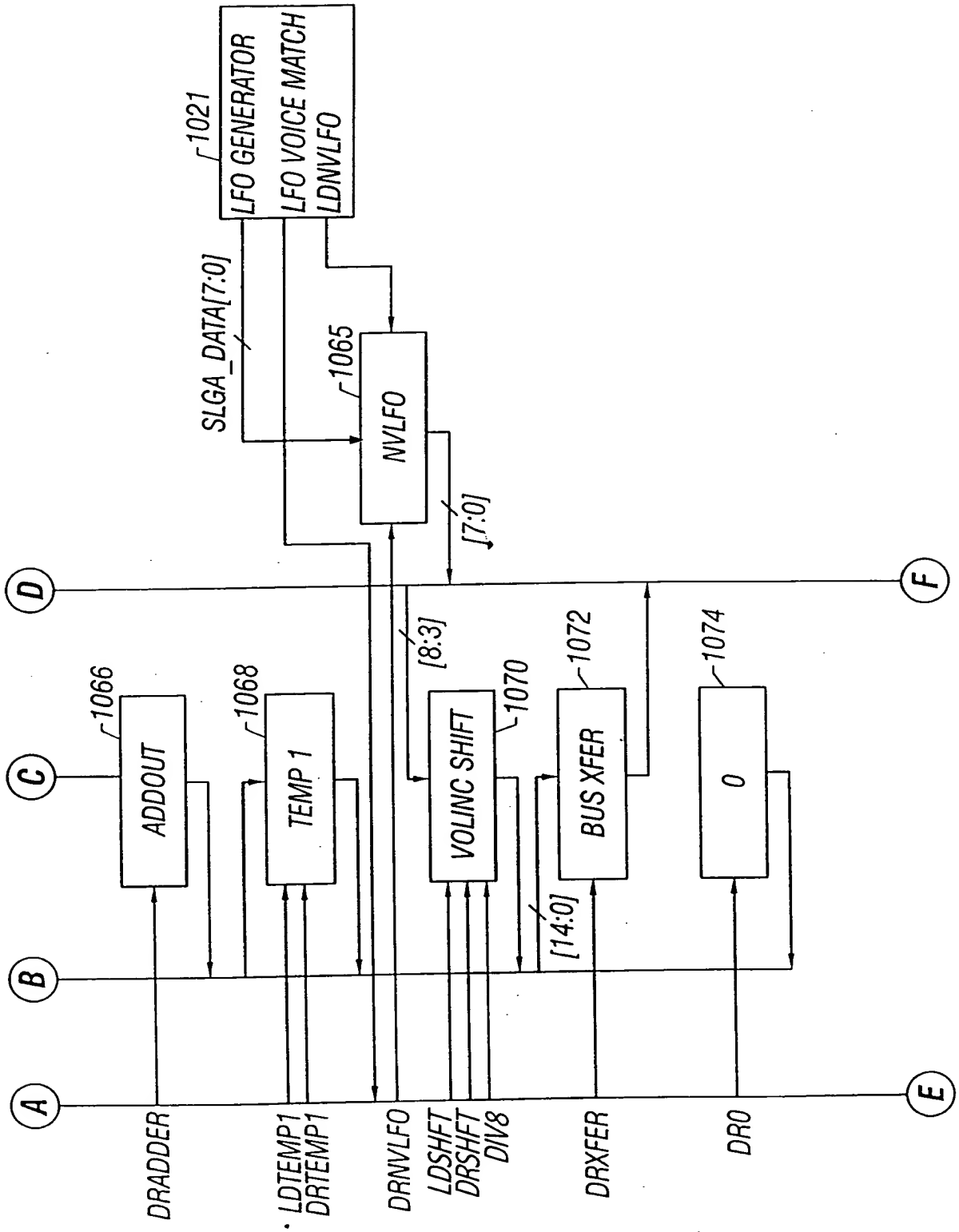

1021
LFO GENERATOR
LFO VOICE MATCH
LDNVLFO
SLGA_DATA[7:0]
1065
NVLFO
[7:0]
D
F
[8:3]
1066
ADDOUT
1068
TEMP 1
1070
VOLINC SHIFT
1072
BUS XFER
1074
0
C
B
[14:0]
A
E
DRADDER
LDTEMP1
DRTEMP1
DRNVLFO
LDSHFT
DRSHFT
DIV8
DRXFER
DR0

FIG. 109B

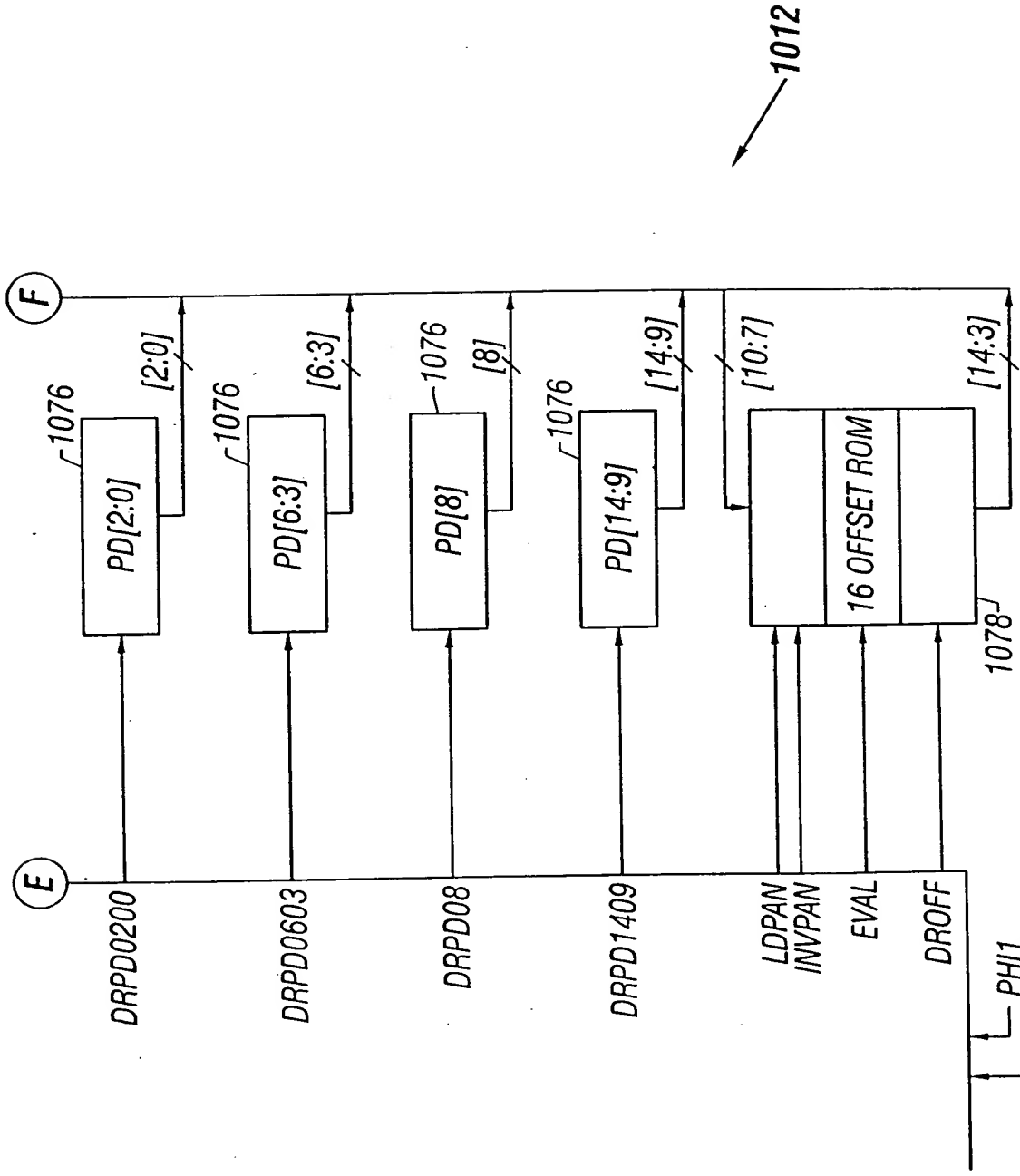

1012
F
E
1076
PD[2:0]
[2:0]
1076
PD[6:3]
[6:3]
1076
PD[8]
[8]
1076
PD[14:9]
[14:9]
[10:7]
16 OFFSET ROM
[14:3]
1078
DRPD0200
DRPD0603
DRPD08
DRPD1409
LDPAN
INVPAN
EVAL
DROFF
PHI1
FR8, FR64

FIG. 109C

Clock #	Result bus	op	Reg. array bus	equation	comments
1			ROFF(PAN)		• start decoding PAN based on OFFEN
2			VLFO		• load register array with next value from LFO generator if LFO voices match
3	sign extended VLFO	+ 17s	VOL	VOL(L)+VLFO	• add volume LFO variation to VOL
4	result=> temp1	+ 15u	-ROFF	VOL(L)+VLFO-ROFF	• ROFF output from ROM or register array based on OFFEN • result can not be grater than 32767 or negative
5	temp1	+ 15u	-LOFF	VOL(L)+VLFO-LOFF	• LOFF output from ROM or register array based on OFFEN • result can not be greater than 32767 or negative
6	temp1 0	+ 15u	[+,-] EVOL	VOL(L)+VLFO-EVOL EVOL	• offset by EVOL or just output EVOL based on SMSI[AEP] • result can not be greater than 32767 or negative

FIG. 110A

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

Clock #	Result bus	op	Reg. array bus	equation	comments
7			VOLINC		
8	[+,-] shifted VOLINC	+ 17s	VOL	VOL± VOLINC	• enable update of VOL based on FR8 or FR64 • shift VOLINC bit field based on rate bits • invert result bus input based on DIR
9	[+,-] (result=> temp1)	+ 17s	[+END, -START]	±(VOL±VOLINC) ±[START,END]	• choose [+END,-START] based on LPE, BLEN,DIR • latch sign of operation
10	[+,-] result	+ 17s	[END, START]	[START,END] ±(±(VOL VOLINC) ±[START,END])	• choose [+,-] and [END, START] based on LPE, BLEN and DIR
11	[result, temp1]		NEXT VOL= result bus		• choose [result, temp1] on the result bus based on latch sign value above • upper bits truncate to get 15 bit unsigned result
12					

FIG. 110B

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

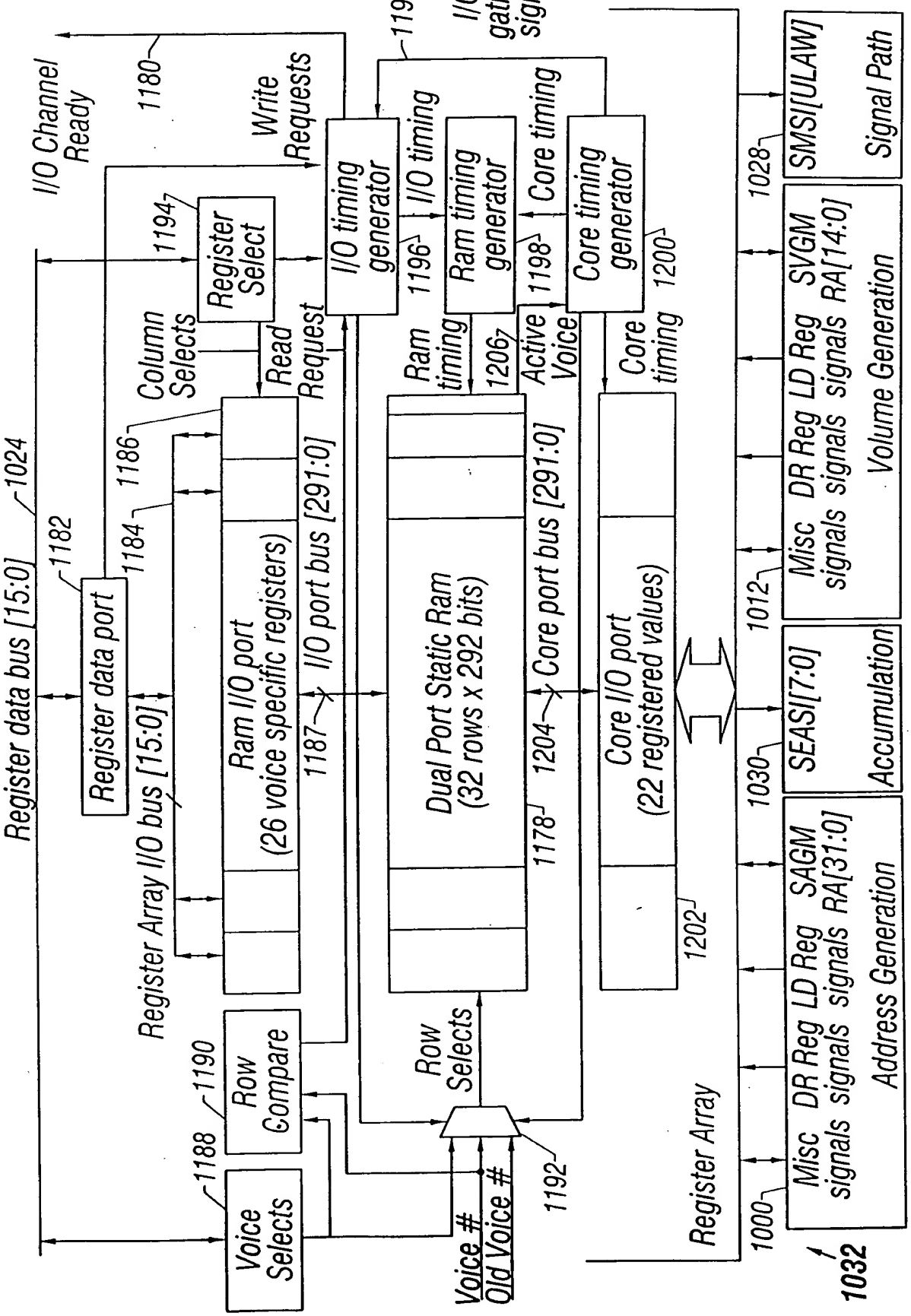

Register data bus [15:0]
1024
1182
Register data port
1184
Register Array I/O bus [15:0]
1186
Column Selects
Register Select
1194
Read Request
Ram I/O port (26 voice specific registers)
I/O port bus [291:0]
1187
Dual Port Static Ram (32 rows x 292 bits)
1178
Core port bus [291:0]
1204
Core I/O port (22 registered values)
1202
Register Array
1188
Voice Selects
1190
Row Compare
Row Selects
1192
Voice #
Old Voice #
I/O Channel Ready
1180
Write Requests
I/O timing generator
1197
I/O gating signal
1196
I/O timing
Ram timing generator
Ram timing
1206
Active Voice
1198
Core timing
Core timing generator
1200
Core timing
1000
Misc DR Reg LD Reg signals signals
SAGM RA[31:0]
Address Generation
1030
SEASI[7:0]
Accumulation
1012
Misc DR Reg LD Reg signals signals
SVGM RA[14:0]
Volume Generation
1028
SMSI[ULAW]
Signal Path
1032

FIG. 111

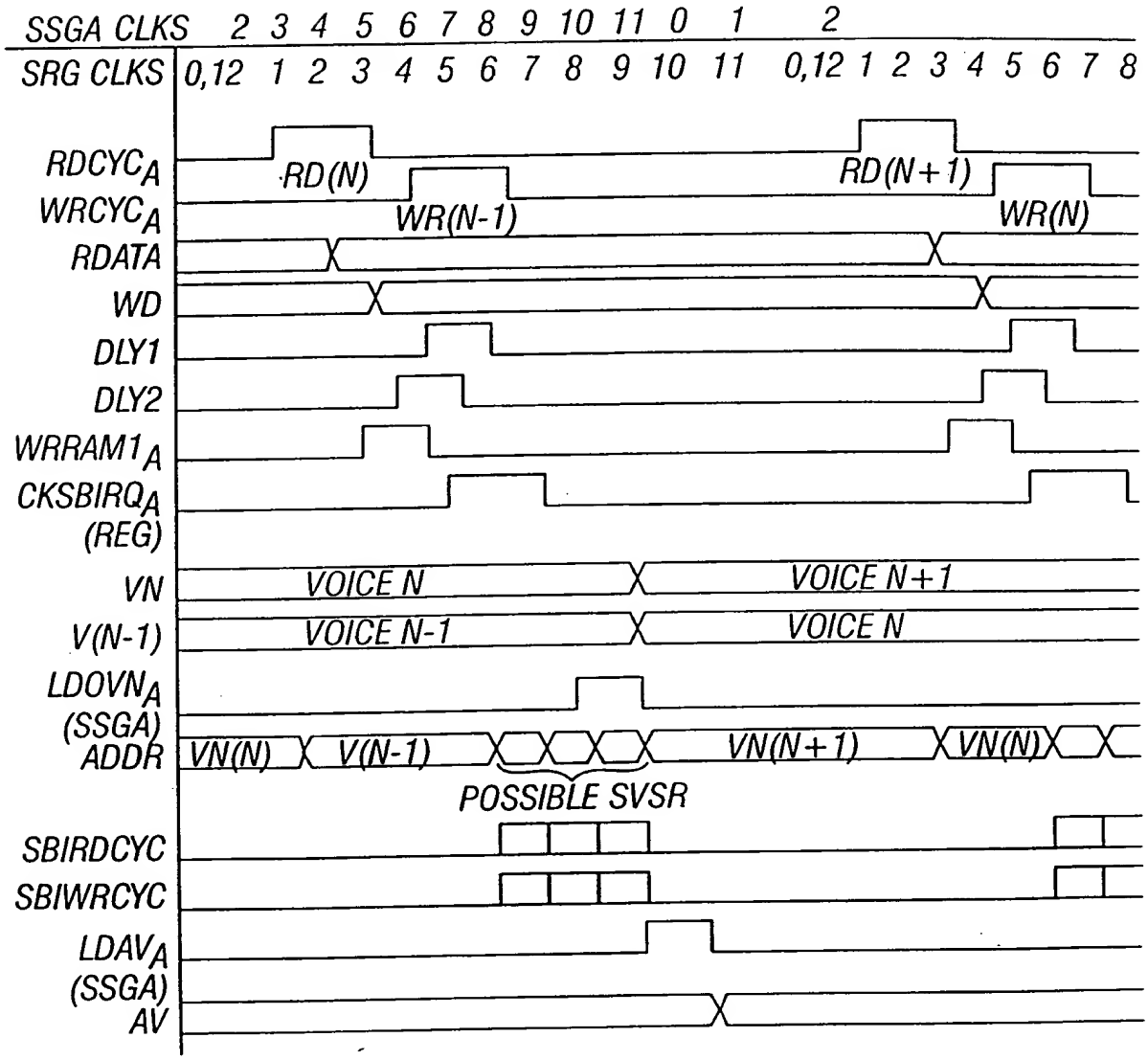

SSGA CLKS 2 3 4 5 6 7 8 9 10 11 0 1 2
SRG CLKS 0,12 1 2 3 4 5 6 7 8 9 10 11 0,12 1 2 3 4 5 6 7 8
RDCYC_A
RD(N)
RD(N+1)
WRCYC_A
WR(N-1)
WR(N)
RDATA
WD
DLY1
DLY2
WRRAM1_A
CKSBIRQ_A
(REG)
VN
VOICE N
VOICE N+1
V(N-1)
VOICE N-1
VOICE N
LDOVN_A
(SSGA)
ADDR
VN(N)
V(N-1)
VN(N+1)
VN(N)
POSSIBLE SVSR
SBIRDCYC
SBIWRCYC
LDAV_A
(SSGA)
AV

FIG. 112

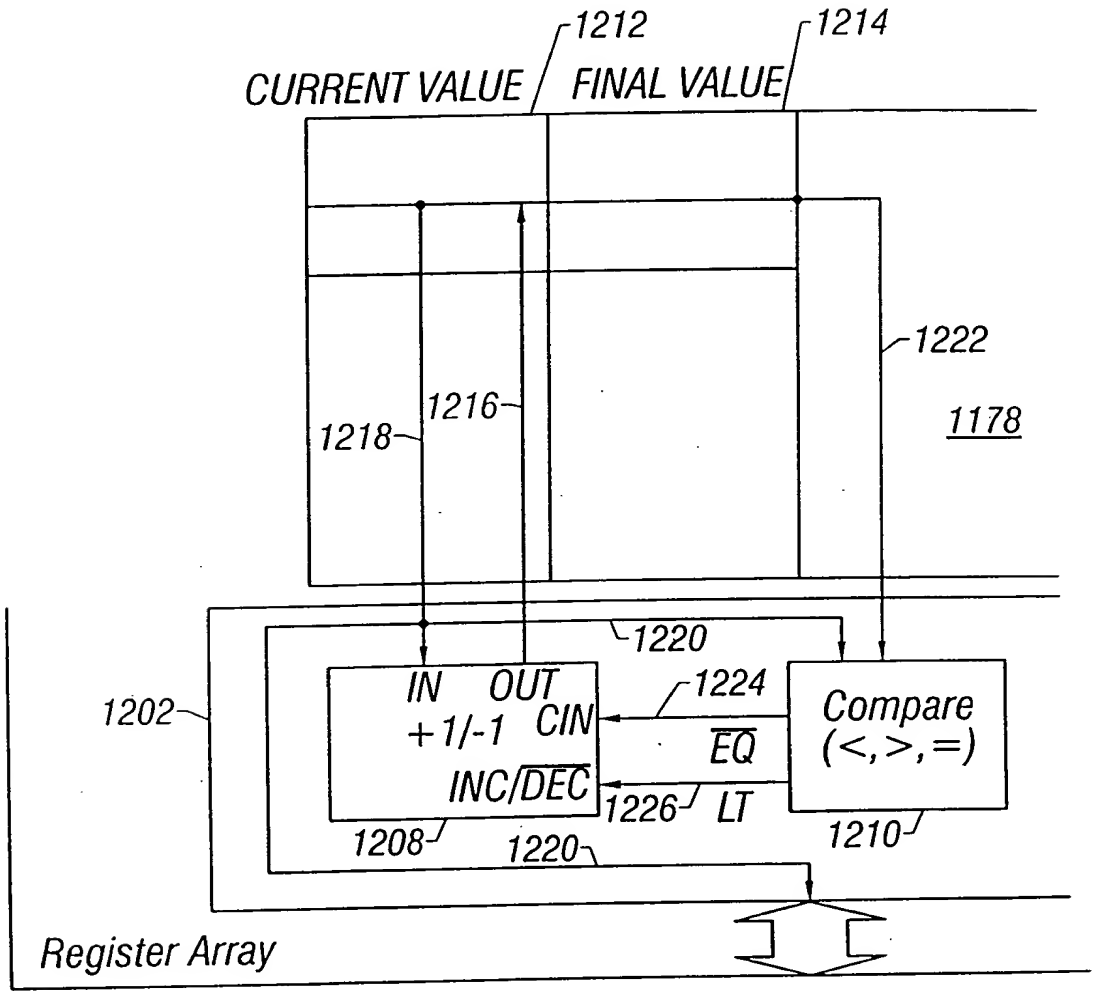

1212
1214
CURRENT VALUE
FINAL VALUE
1222
1178
1216
1218
1220
1202
IN OUT
+1/-1 CIN
INC/DEC
1224
EQ
1226
LT
Compare
(<,>,=)
1208
1220
1210
Register Array
1032

FIG. 113

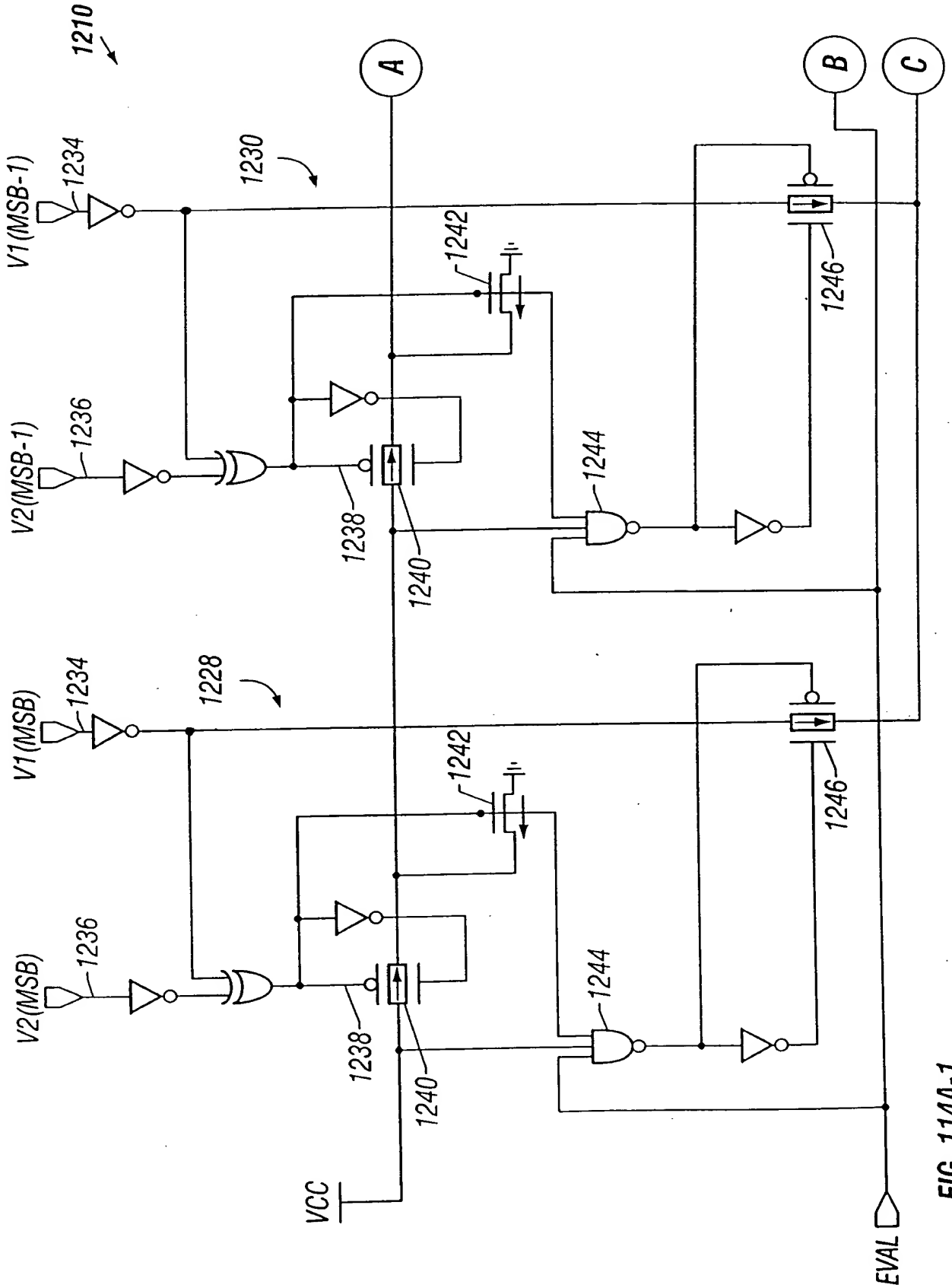

1210
A
B
C
V1(MSB-1)
1234
1230
1242
1246
V2(MSB-1)
1236
1244
1238
1240
V1(MSB)
1234
1228
1242
1246
V2(MSB)
1236
1244
1238
1240
VCC
EVAL

FIG. 114A-1

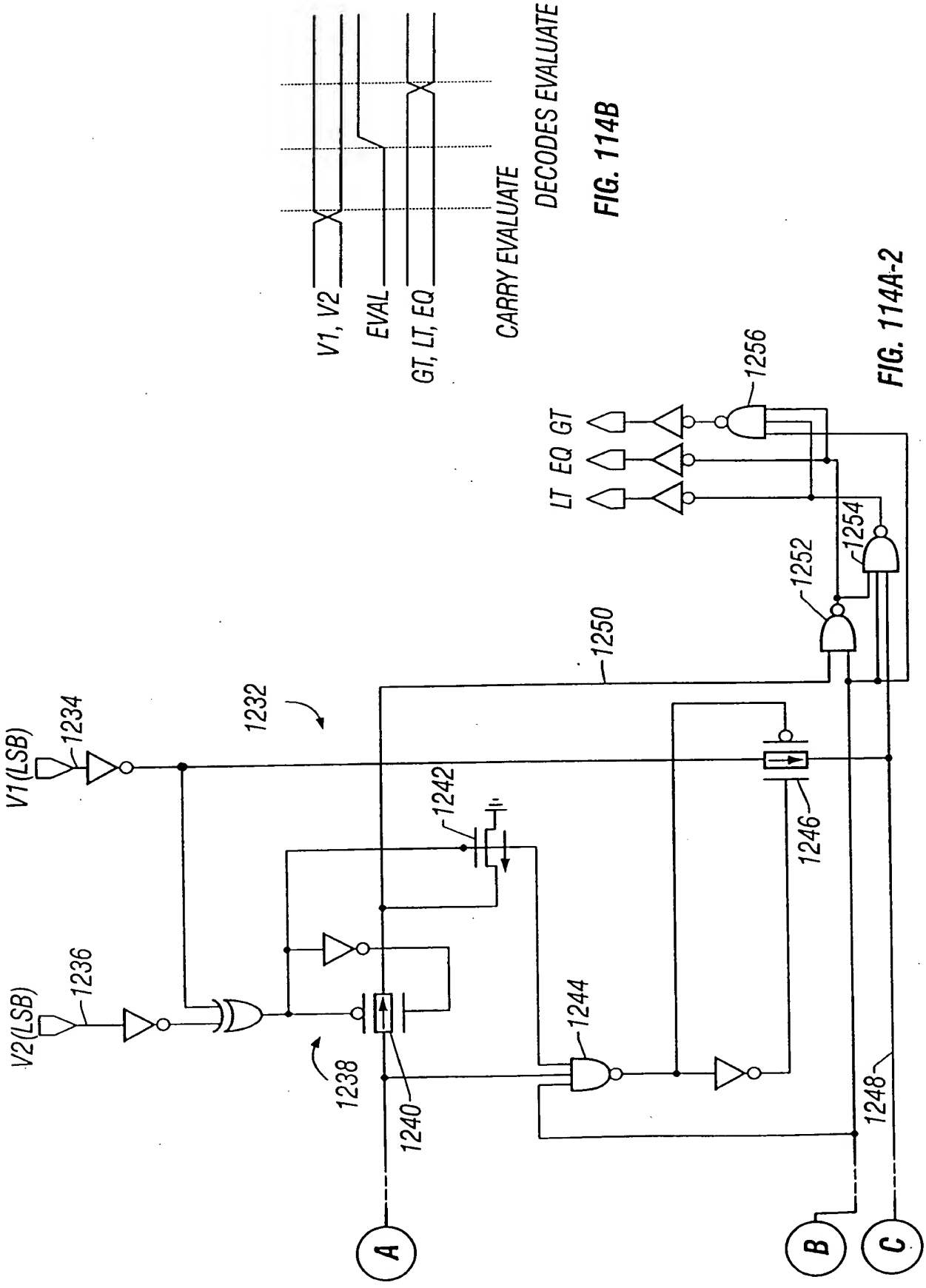


FIG. 114B

FIG. 114A-2

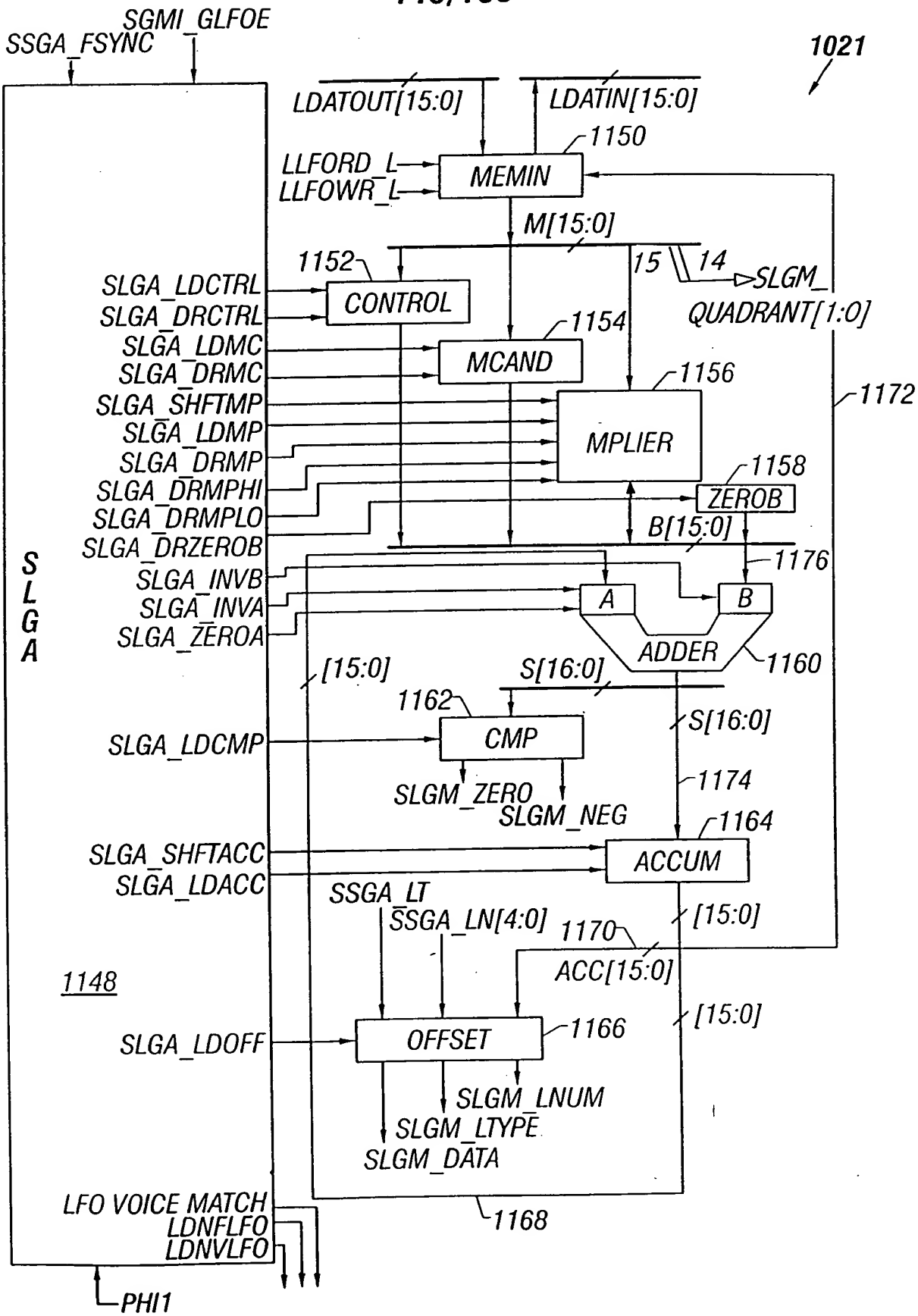

SGMI_GLFOE
SSGA_FSYNC
1021
LDATOUT[15:0]
LDATIN[15:0]
1150
LLFORD_L
LLFOWR_L
MEMIN
M[15:0]
1152
15
14
SLGM_
QUADRANT[1:0]
SLGA_LDCTRL
SLGA_DRCTRL
CONTROL
1154
SLGA_LDMC
SLGA_DRMC
MCAND
1156
1172
SLGA_SHFTMP
SLGA_LDMP
SLGA_DRMP
SLGA_DRMPHI
SLGA_DRMPLO
MPLIER
1158
ZEROB
B[15:0]
SLGA_DRZEROB
1176
SLGA_INVB
SLGA_INVA
SLGA_ZEROA
A
B
ADDER
1160
S
L
G
A
[15:0]
S[16:0]
1162
S[16:0]
SLGA_LDCMP
CMP
1174
SLGM_ZERO
SLGM_NEG
1164
SLGA_SHFTACC
SLGA_LDACC
ACCUM
SSGA_LT
SSGA_LN[4:0]
[15:0]
1170
ACC[15:0]
1148
[15:0]
SLGA_LDOFF
OFFSET
1166
SLGM_LNUM
SLGM_LTYPE
SLGM_DATA
LFO VOICE MATCH
LDNFLFO
LDNVLFO
1168
PHI1

FIG. 115

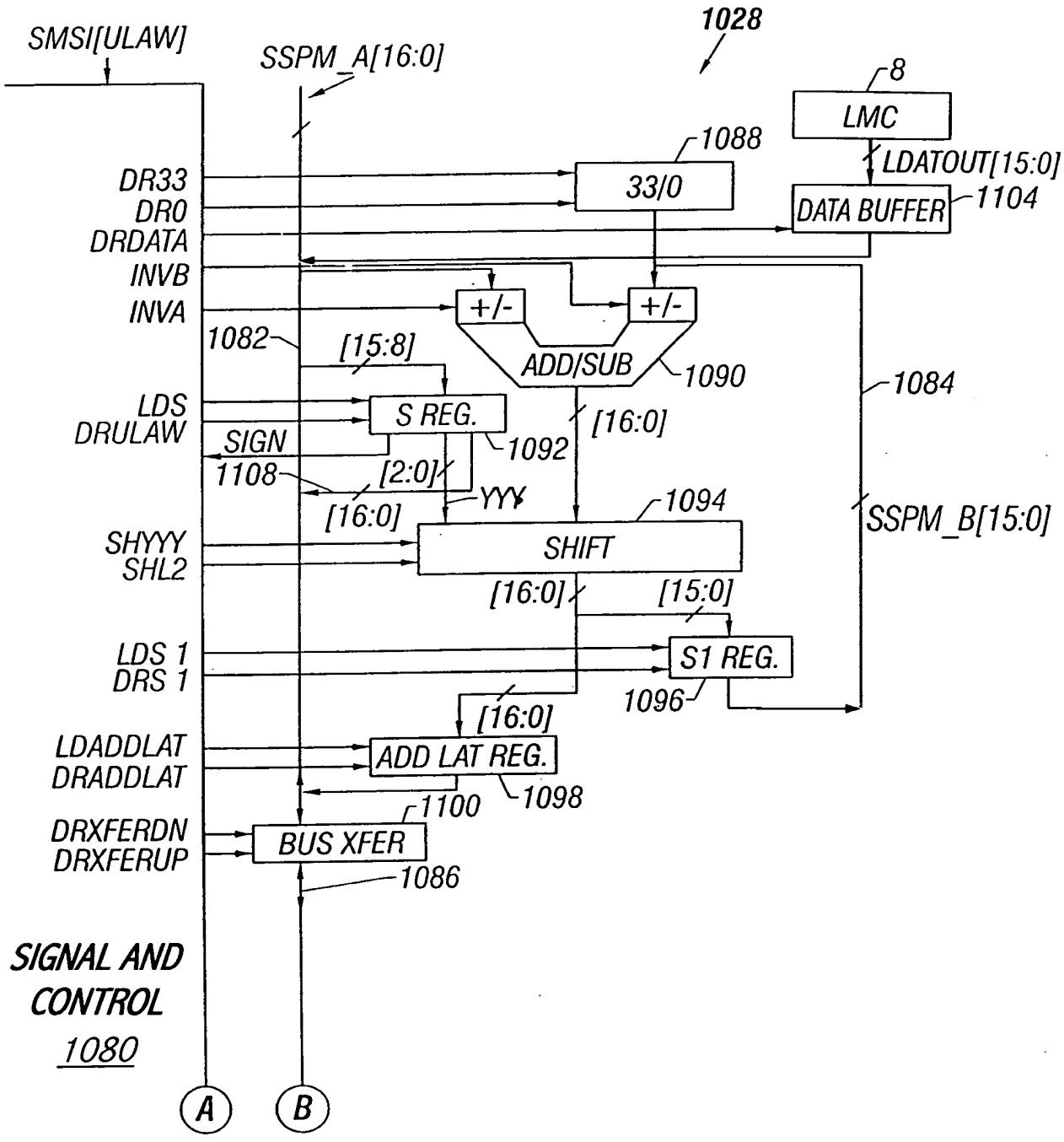

SMSI[ULAW]
SSPM_A[16:0]
1028
8
LMC
1088
LDATOUT[15:0]
DR33
DR0
DRDATA
33/0
DATA BUFFER
1104
INVB
INVA
+/-
+/-
ADD/SUB
1090
1082
[15:8]
1084
LDS
DRULAW
S REG.
[16:0]
SIGN
1108
1092
[2:0]
YYY
[16:0]
1094
SSPM_B[15:0]
SHYYY
SHL2
SHIFT
[16:0]
[15:0]
LDS 1
DRS 1
S1 REG.
1096
[16:0]
LDADDLAT
DRADDLAT
ADD LAT REG.
1098
1100
DRXFERDN
DRXFERUP
BUS XFER
1086
SIGNAL AND
CONTROL
1080
A
B

FIG. 116A

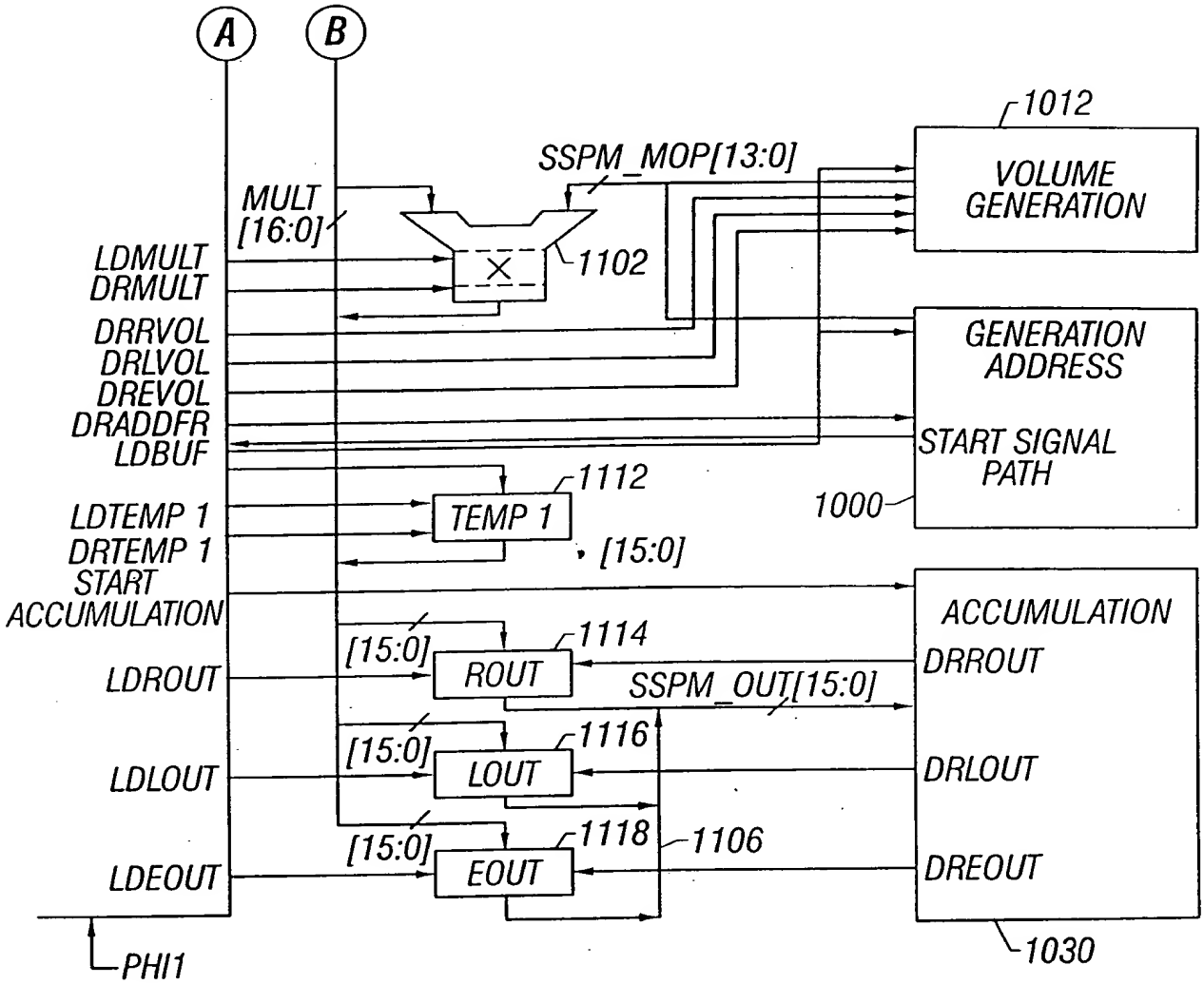
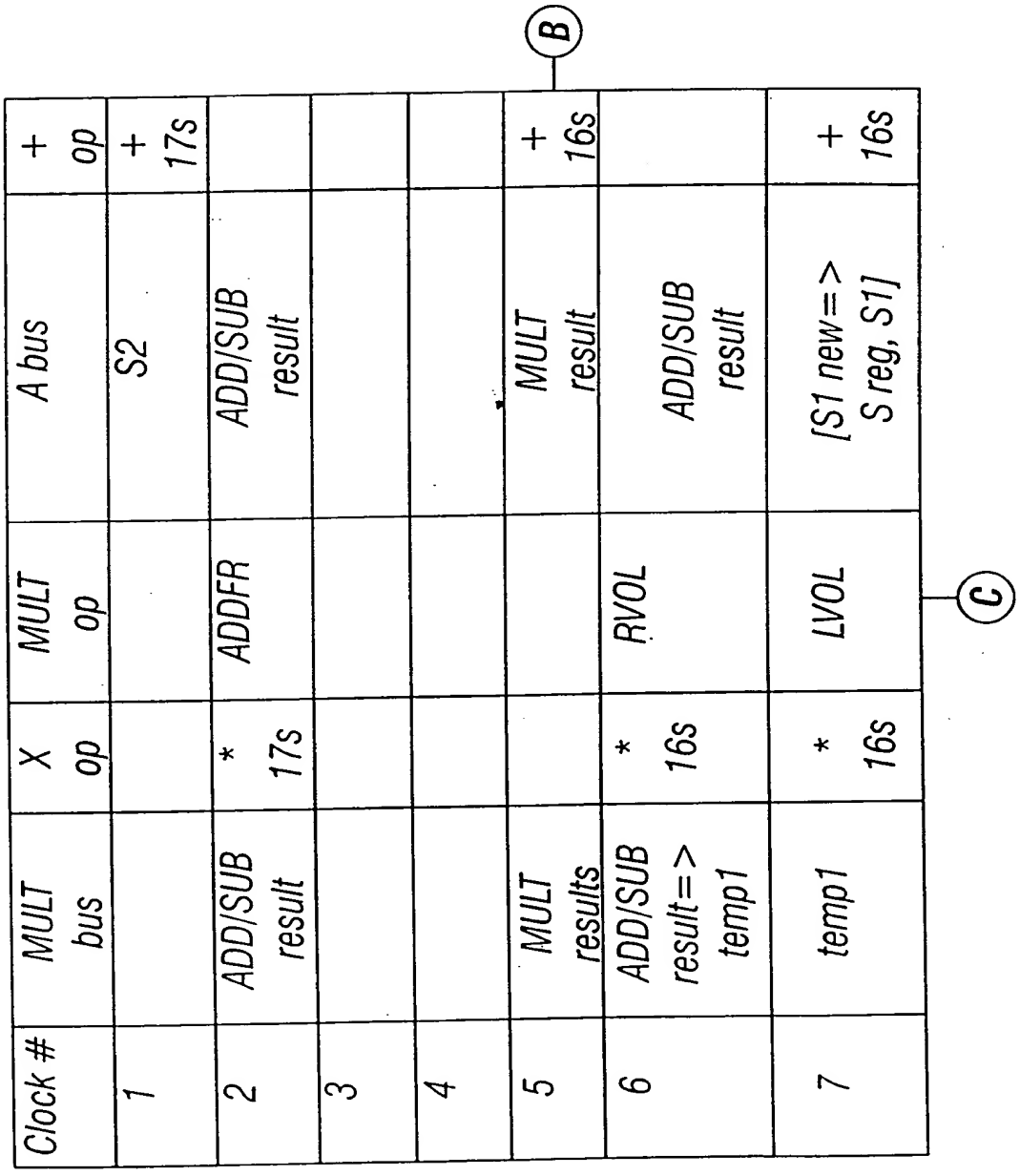

A
B
1012
SSPM_MOP[13:0]
VOLUME
GENERATION
MULT
[16:0]
LDMULT
DRMULT
X
1102
DRRVOL
DRLVOL
DREVOL
DRADDFR
LDBUF
GENERATION
ADDRESS
START SIGNAL
PATH
1000
1112
LDTEMP 1
DRTEMP 1
TEMP 1
[15:0]
START
ACCUMULATION
ACCUMULATION
[15:0]
1114
LDROUT
ROUT
DRROUT
SSPM_OUT[15:0]
[15:0]
1116
LDLOUT
LOUT
DRLOUT
[15:0]
1118
1106
LDEOUT
EOUT
DREOUT
PHI1
1030

FIG. 116B



Clock #	MULT bus	X op	MULT op	A bus	+ op
1				S2	+ 17s
2	ADD/SUB result	* 17s	ADDFR	ADD/SUB result	
3					
4					
5	MULT results			MULT result	+ 16s
6	ADD/SUB result=> temp1	* 16s	RVOL	ADD/SUB result	
7	temp1	* 16s	LVOL	[S1 new=> S reg, S1]	+ 16s

FIG. 117A

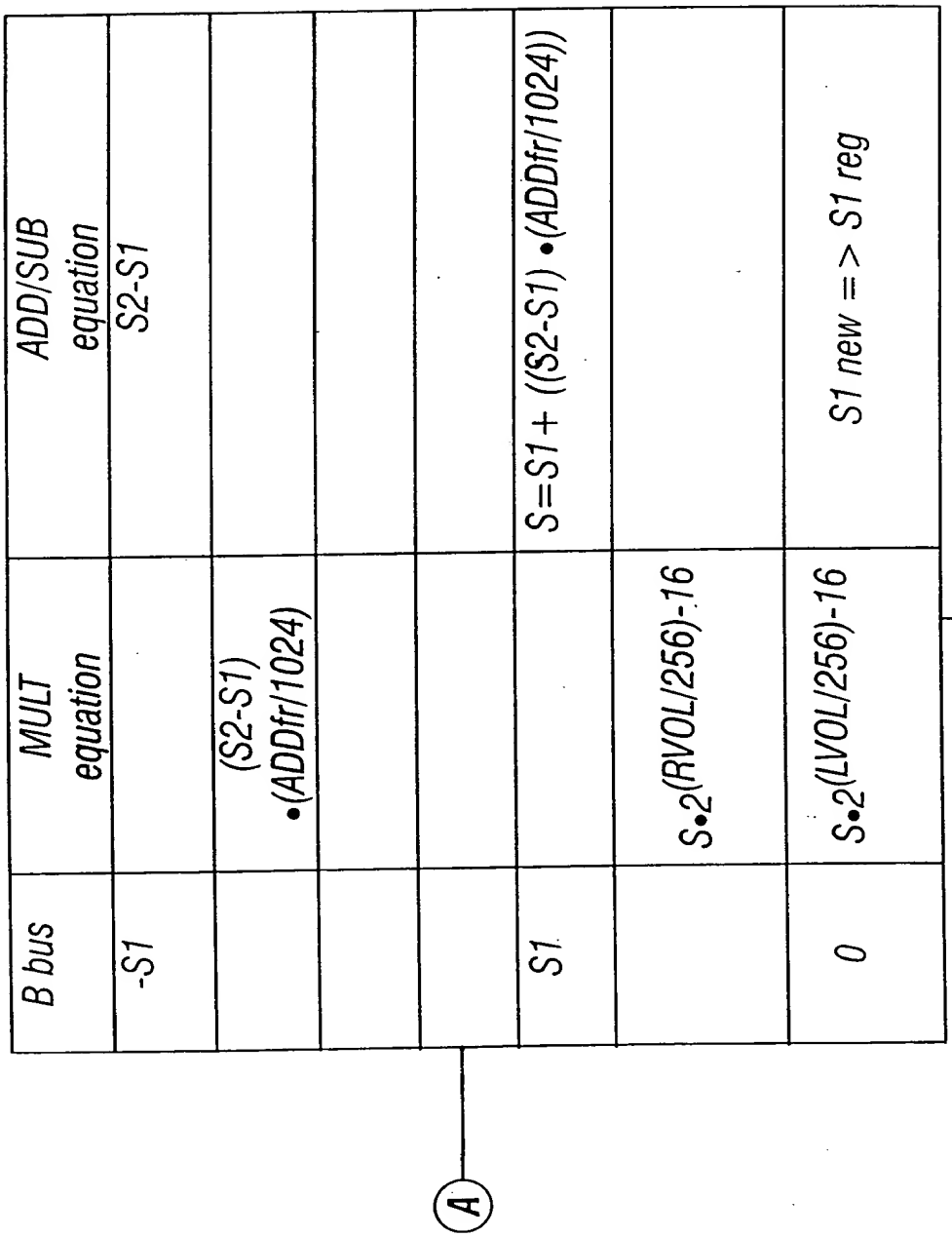

B bus
MULT equation
ADD/SUB equation
-S1
S2-S1
(S2-S1) •(ADDfr/1024)
S=S1+ ((S2-S1) •(ADDfr/1024))
S•2(RVOL/256)-16
0
S•2(LVOL/256)-16
S1 new = > S1 reg
A
D

FIG. 117B

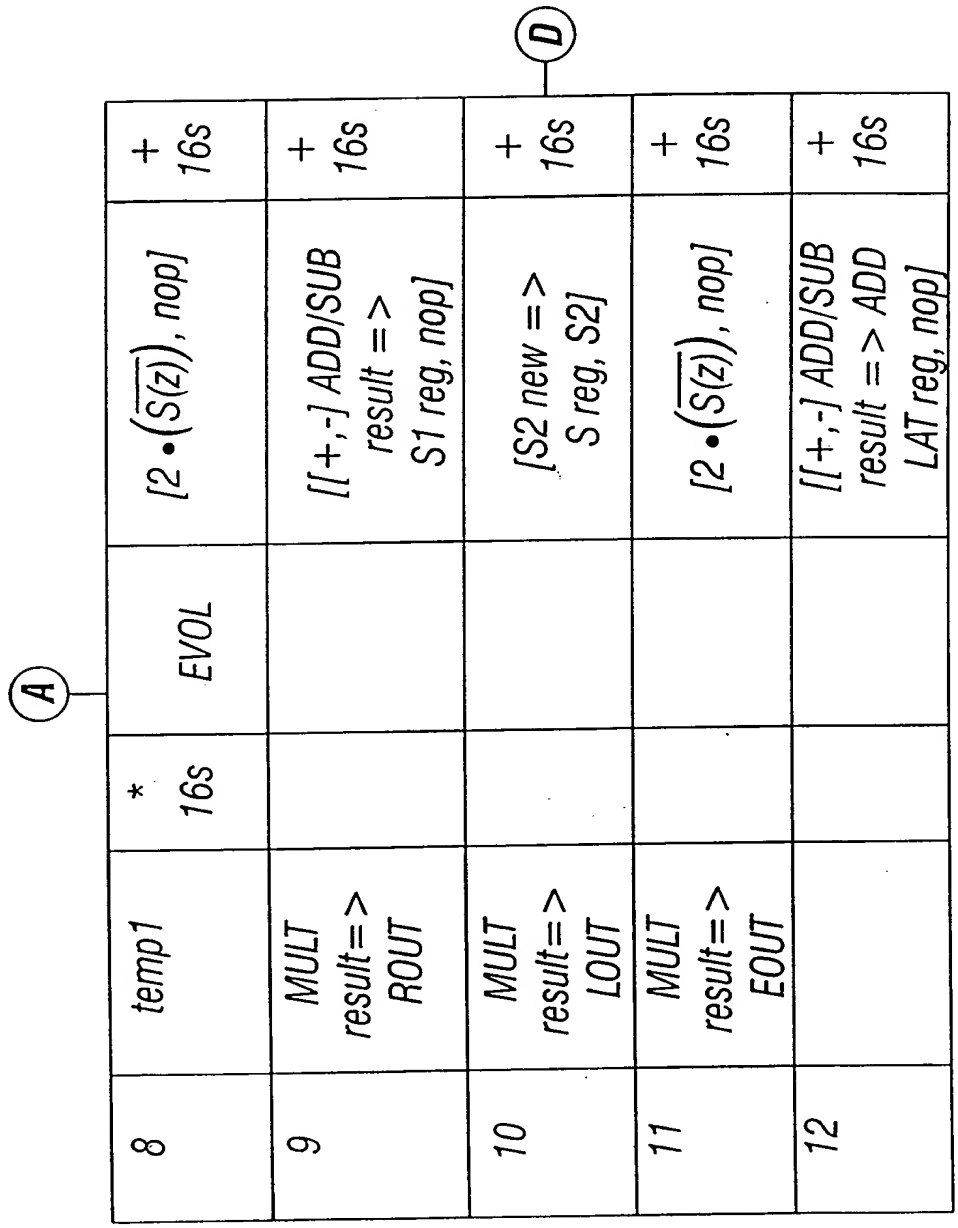
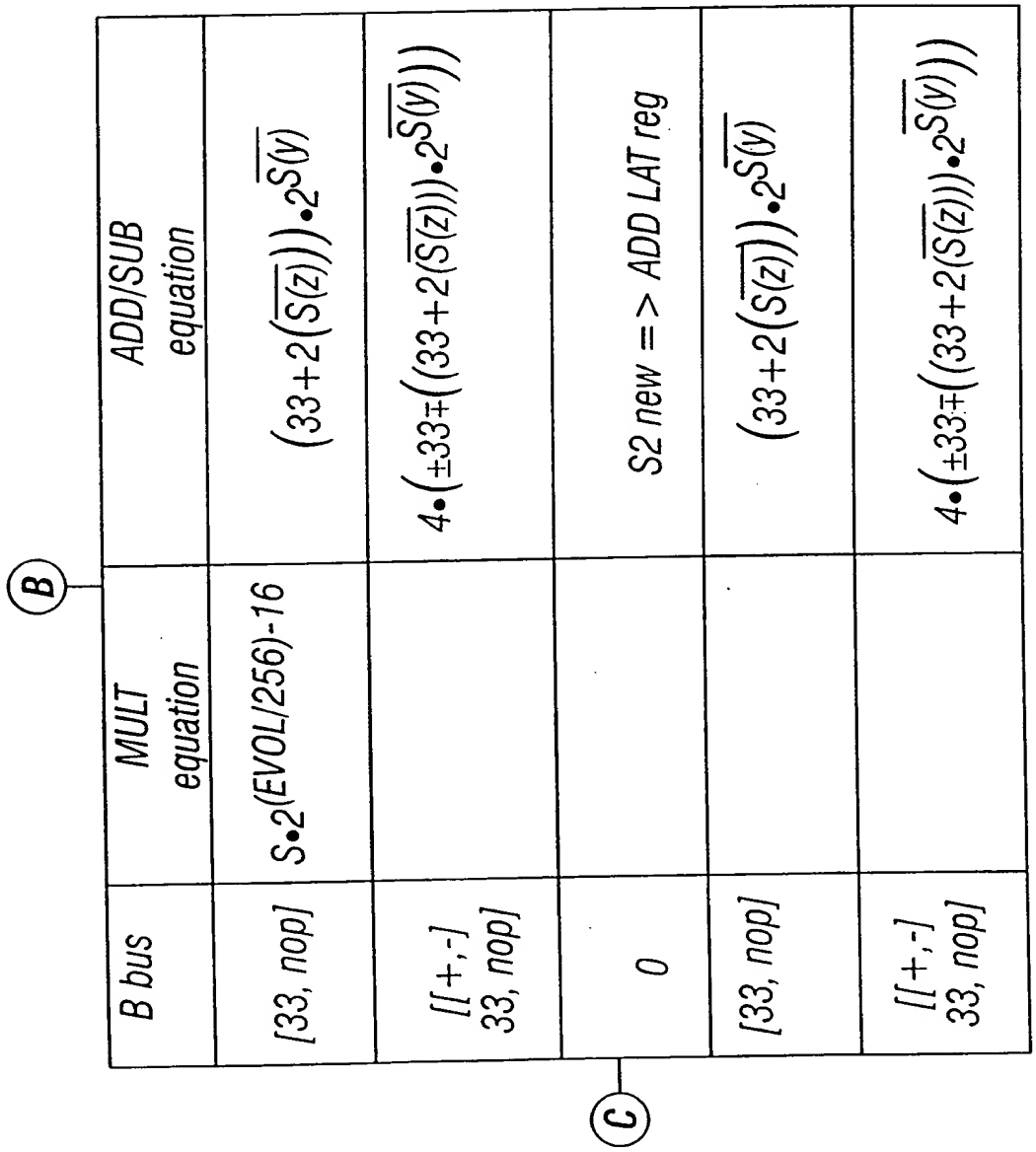

A
D
8
temp1
*
16s
EVOL
[2 • (S(z)), nop]
+
16s
9
MULT
result=>
ROUT
[[+,-] ADD/SUB
result =>
S1 reg, nop]
+
16s
10
MULT
result=>
LOUT
[S2 new =>
S reg, S2]
+
16s
11
MULT
result=>
EOUT
[2 • (S(z)), nop]
+
16s
12
[[+,-] ADD/SUB
result => ADD
LAT reg, nop]
+
16s

FIG. 117C



B bus	MULT equation	ADD/SUB equation
[33, nop]	$S \bullet 2^{(EVOL/256)-16}$	$\left(33+2\left(\overline{S(z)}\right)\right) \bullet 2^{\overline{S(y)}}$
[[+,-] 33, nop]		$4 \bullet \left(\pm 33 \mp \left((33+2\overline{(S(z))}) \bullet 2^{\overline{S(y)}}\right)\right)$
0		S2 new => ADD LAT reg
[33, nop]		$\left(33+2\left(\overline{S(z)}\right)\right) \bullet 2^{\overline{S(y)}}$
[[+,-] 33, nop]		$4 \bullet \left(\pm 33 \mp \left((33+2\overline{(S(z))}) \bullet 2^{\overline{S(y)}}\right)\right)$

FIG. 117D

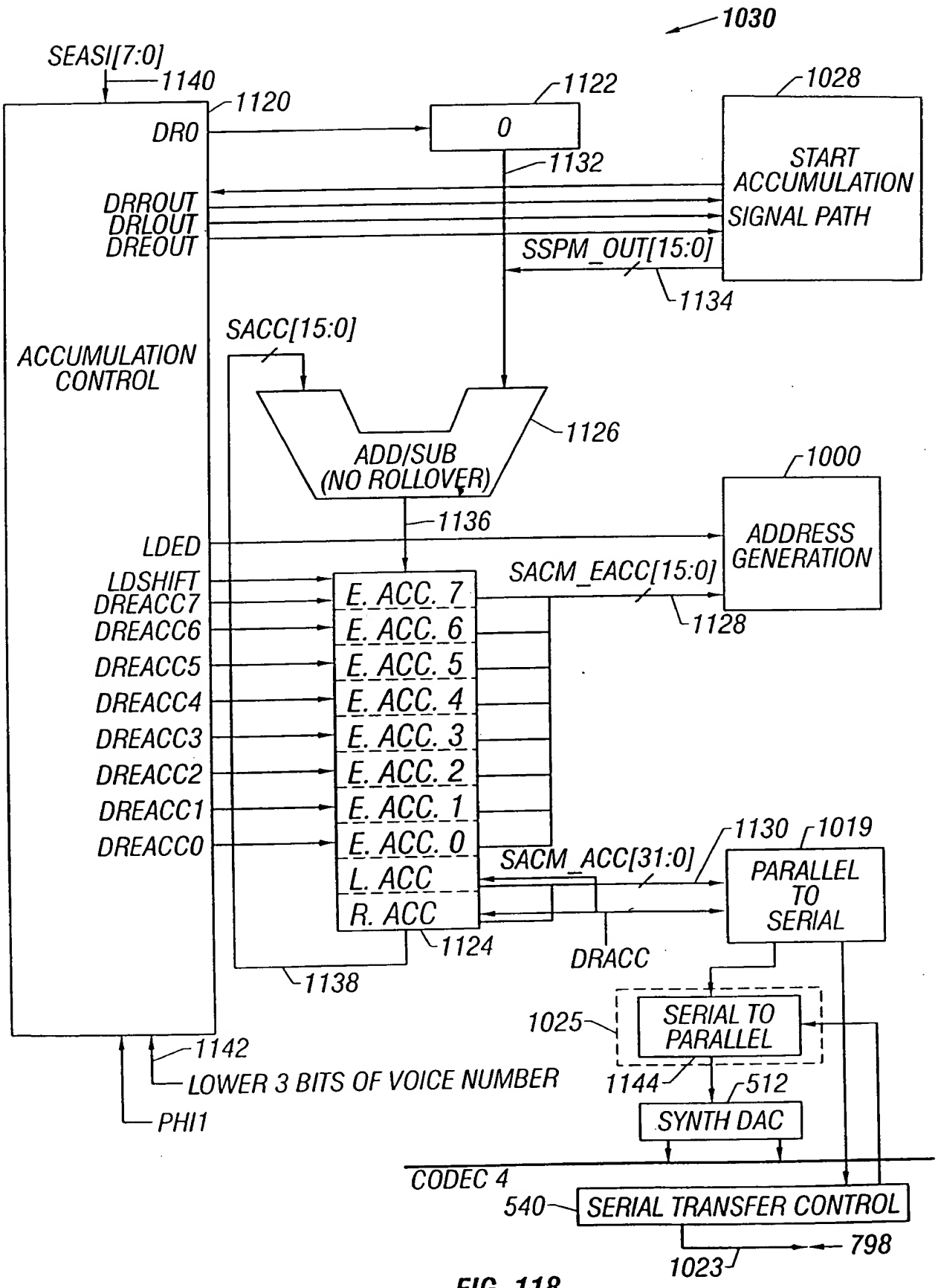

1030
SEASI[7:0]
1140
1120
DR0
1122
0
1028
START ACCUMULATION SIGNAL PATH
1132
DRROUT
DRLOUT
DREOUT
SSPM_OUT[15:0]
1134
SACC[15:0]
ACCUMULATION CONTROL
1126
ADD/SUB (NO ROLLOVER)
1000
ADDRESS GENERATION
1136
LDED
LDSHIFT
DREACC7
DREACC6
DREACC5
DREACC4
DREACC3
DREACC2
DREACC1
DREACC0
E. ACC. 7
E. ACC. 6
E. ACC. 5
E. ACC. 4
E. ACC. 3
E. ACC. 2
E. ACC. 1
E. ACC. 0
L. ACC
R. ACC
SACM_EACC[15:0]
1128
1130
1019
SACM_ACC[31:0]
PARALLEL TO SERIAL
1124
DRACC
1138
1025
SERIAL TO PARALLEL
1142
LOWER 3 BITS OF VOICE NUMBER
1144
512
SYNTH DAC
PHI1
CODEC 4
540
SERIAL TRANSFER CONTROL
798
1023

FIG. 118

Clock #		op		equation	comments
1	R.ACC	+	ROUT	R.ACC. = R.ACC.+ROUT	
2	L.ACC	+	LOUT	L.ACC. = L.ACC.+LOUT	
3	E.ACC.0	+	[EOUT,0]	E.ACC.0 = E.ACC.0+[EOUT,0]	• EOUT or 0 is added based on SEASI[0]
4	E.ACC.1	+	[EOUT,0]	E.ACC.1 = E.ACC.1+[EOUT,0]	• EOUT or 0 is added based on SEASI[1]
5	E.ACC.2	+	[EOUT,0]	E.ACC.2 = E.ACC.2+[EOUT,0]	• EOUT or 0 is added based on SEASI[2]
6	E.ACC.3	+	[EOUT,0]	E.ACC.3 = E.ACC.3+[EOUT,0]	• EOUT or 0 is added based on SEASI[3]
7	E.ACC.4	+	[EOUT,0]	E.ACC.4 = E.ACC.4+[EOUT,0]	• EOUT or 0 is added based on SEASI[4]
8	E.ACC.5	+	[EOUT,0]	E.ACC.5 = E.ACC.5+[EOUT,0]	• EOUT or 0 is added based on SEASI[5]
9	E.ACC.6	+	[EOUT,0]	E.ACC.6 = E.ACC.6+[EOUT,0]	• EOUT or 0 is added based on SEASI[6]
10	E.ACC.7	+	[EOUT,0]	E.ACC.7 = E.ACC.7+[EOUT,0]	• EOUT or 0 is added based on SEASI[7]
11					• if voice is an effects voice output appropriate effects accumulator based on lower 3 bits of voice number • on 32nd voice output R and L accummulators
12					

FIG. 119

App. No. 09/352,659
Dkt. No. 028-0128-3
Inv.: David Norris
Att'y: Mark Zagorin (512)338-6300

SSG	SRG	SAG	SVG
LFSYNC			
0.12. FSYNC			
1. AV(in)			
2	0,12		
3	1. RD0		
4	2. RD0		
5	3	0.12	0.12
6	4	1. NFLFO(in)	1
7	5. WR31*	2	2. NVLFO(in)
8	6. WR31*	3. ADD(out) ADDfr(out)0	3
9	7	4	4
10	8	5	5. RVOL(out)0
11	9	6	6. LVOL(out)0
0,12. VN(out)	10	7. START(out)	7. EVOL(out)0
1. AV(in)	11	8	8
2	0.12	9. EADD(out)0	9
3	1. RD1	10	10
4	2. RD1	11	11
5	3	0.12	0.12
6	4	1. NFLFO(in)	1
7	5 *WRO*	2	2. NVLFO(in)
8	6 *WRO*	3. ADD(out) ADDfr(out)1	3
9	7	4	4
10	8	5	5. RVOL(out)1
11	9	6	6. LVOL(out)1
0.12. VN(out)	10	7. START(out)	7. EVOL(out)1

FIG. 120A

*NOT DONE AFTER RESET

1. AV(in)	11	8	8
2	0.12	9. EADD(out)1	9
3	1. RD2	10	10
4	2. RD2	11	11
5	3	0.12	0.12
6	4	1. NFLFO(in)	1
7	5. WR1	2	2. NVLFO(in)
8	6. WR1	3. ADD(out) ADDfr(out)2	3
9	7	4	4
10	8	5	5. RVOL(out)2
11	9	6	6. LVOL(out)2
0.12. VN(out)	10	7. START(out)	7. EVOL(out)2
1. AV(in)	11	8	8
2	0.12	9. EADD(out)2	9
3	1. RD3	10	10
4	2. RD3	11	11
5	3	0.12	0.12
6	4	1. NFLFO(in)	1
7	5. WR2	2	2. NVLFO(in)
8	6. WR2	3. ADD(out) ADDfr(out)3	3
9	7	4	4
10	8	5	5. RVOL(out)3
11	9	6	6. LVOL(out)3
0.12. VN(out)	10	7. START(out)	7. EVOL(out)3
1. AV(in)	11	8	8

FIG. 120B

REPLACEMENT SHEET

SSP	SAC	LMC
		syn1
		2
		3
		4
		o,e1
		2
		3
		4
		syn1
		2
		3. ADD(in)
		4
0.12		syn1
1		2
2. ADDfr(in)31*		3. [ADD+1(in). START(in)]
3		4
4		o,e1
5		2. S1(out)
6. RVOL(in)31*		3
7. LVOL(in)31* S1(in)	B	4
8. EVOL(out)31*		syn1
9. ROUT(out)31*	0.12	2. S2(out)
10. LOUT(out)31* S2(in)	1. ROUT(in)31	3. ADD (in)
11. EOUT(out)31*	2. LOUT(in)31	4
0,12	3. EOUT(in)31	syn1
1	4	2

FIG. 120C

REPLACEMENT SHEET

2. ADDfr(in)0	5	3. [ADD+1(in), START(in)]
3	6	4
4	7	o,e1
5	8	2. S1(out)
6. RVOL(in)0	9	3
7. LVOL(in)0 S1(in)	10	4
8. EVOL(in)0	11. R&Lacc(out) EACC(out)31	syn1
9. ROUT(out)0	0.12	2. S2(out)
10. LOUT(out)0 S2(in)	1. ROUT(in)0	3. ADD(in)
11. EOUT(out)0	2. LOUT(in)0	4
0.12	3. EOUT(in)0	syn1
1	4	2
2. ADDfr(in)1	5	3. [ADD+1(in), START(in)]
3	6	4
4	7	o,e1
5	8	2. S1(out)
6. RVOL(in)1	9	3
7. LVOL(in)1 S1(in)	10	4
8. EVOL(in)1	11. EACC(out)0	syn1
9. ROUT(out)1	0.12	2. S2(out)
10. LOUT(out)1 S2(in)	1. ROUT(in)1	3. ADD(in)
11. EOUT(out)1	2. LOUT(in)1	4
0,12	3. EOUT(in)1	syn1
1	4	2
2. ADDfr(in)2	5	3. [ADD+1(in), START(in)]

A

FIG. 120D

REPLACEMENT SHEET

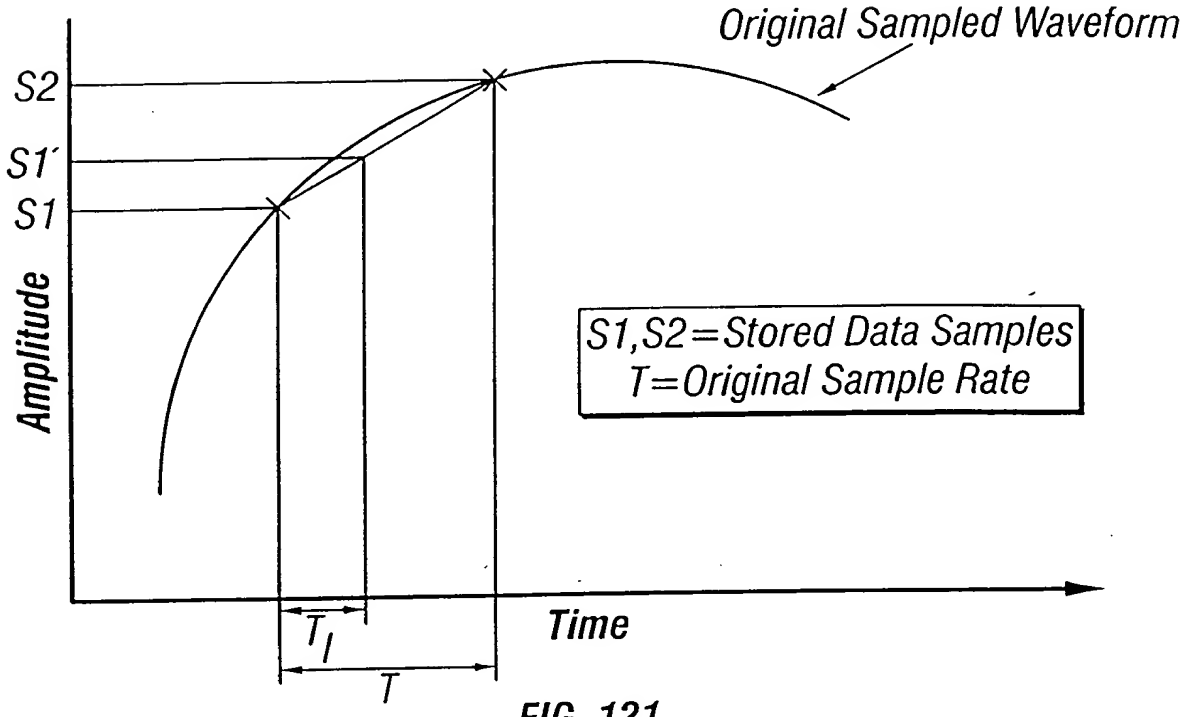


FIG. 121
(Prior Art)

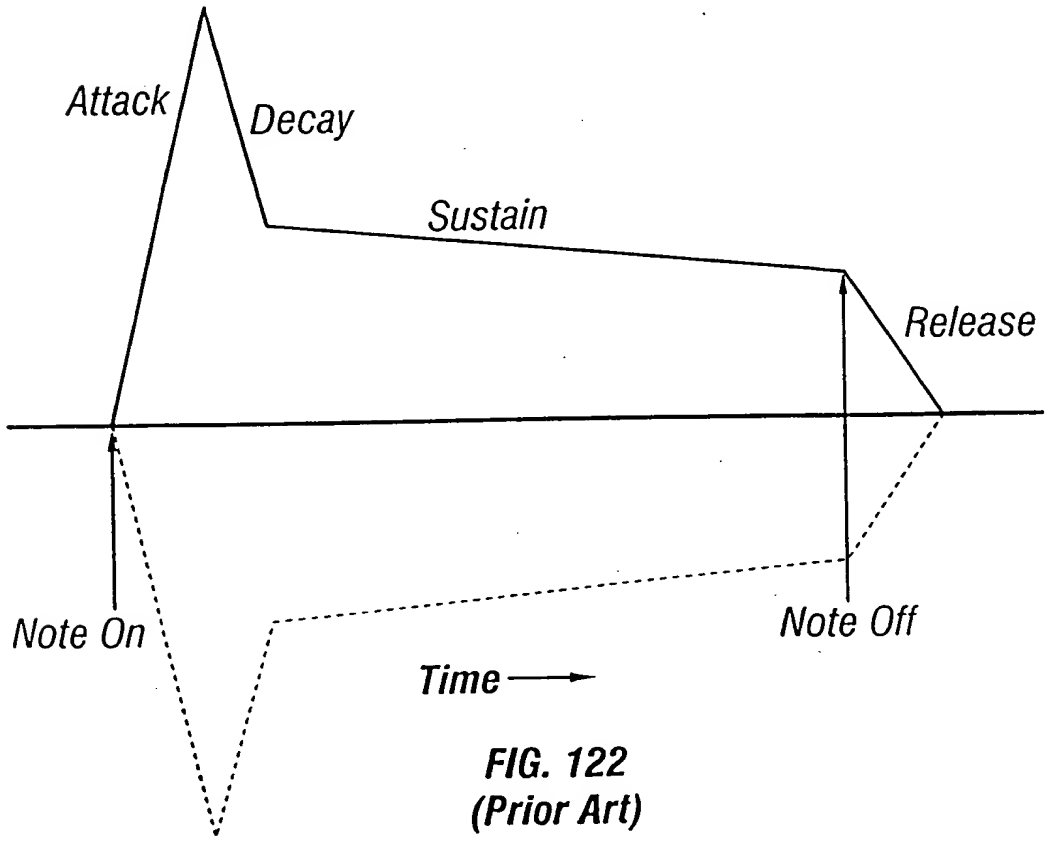


FIG. 122
(Prior Art)